Reconfigurable Advanced Rapid-prototyping Environment (RARE):
A Computing Technology for Challenging Form Factors

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Outline

• Background

• Overview of RARE Architecture
  – Approach
  – Features
  – Software and Programming Model
  – Packaging

• Application Examples

• Summary
Background

• Ideal high performance computing environment is heterogeneous
  – Variety of processing technologies
    • General purpose / multi-core
    • Field Programmable Gate Arrays (FPGAs)
    • Graphics processors
    • Application Specific Integrated Circuits (ASICs)
  – Enables engineer to optimize solution to fit Size, Weight, and Power (SWaP) budget

• Technologies represent different points in trade space
  – Computing horsepower
  – Power consumption
  – Programmability
Background

• Heterogeneous computing approaches have traditionally relied on backplanes
  – Added weight, size, and cost
  – Constrain incremental scalability

• Backplanes limit designer’s ability to realize solutions in physical volumes not conducive to legacy form factors
A New Approach

• MDA funded an SBIR Phase I and II program to address challenges of modularity, scalability, and heterogeneity in deployments with challenging form factors
  – RARE: Reconfigurable Advanced Rapid-prototyping Environment
  – Executed by CEI under technical guidance and influence of NRL, NSWC, and ONR
  – Recipient of 2011 Tibbetts Award
  – No Backplane!

• Presentation will describe architecture and provide real-world application examples
MOSA Inspired Technology

- Decomposes a system into functional COTS building blocks
- Blocks provide a modular way to achieve loosely coupled common operational subsystem components
- When tied together using well defined interfaces, blocks form a complete, scalable processing and control system
RARE Modularity and Scalability

- 6.25” x 6.25” cards with interface connections in three dimensions
  - I/O bandwidth of 39 GB/sec per module via PCIe, LVDS, and SerDes
  - 3D direct connectivity of FPGA processing elements
  - I²C network of microcontrollers for health and status management
- Stack and/or tile modules in x, y, and z
  - Incrementally scale performance, I/O bandwidth, and physical footprint
  - Physically reconfigure systems while maintaining common HW/FW/SW
  - Solutions in a fraction of the volume of traditional backplanes
COTS Modules: Digital and RF

**GP/FPGA Processor**
- AMCC 460SX PowerPC
- Xilinx Virtex-6 FPGA
- Dual 1Gb Ethernet
- USB, RS-232

**ADC+Processor**
- 10 ADC channels
- 16b @ 160MSPS
- Xilinx Virtex-6 FPGA

**DAC+Processor**
- 2 DAC channels
- 16b @ 1GSPS
- Xilinx Virtex-6 FPGA

**Starter Kit**
- TRL 8

**Roadmap**
- Stratix V
- Multicore GP
- GPU + x86
- Ultra-wideband ADCs
- Enhanced Tamper Resistance

**High Fidelity, Low Phase Noise Clock Distribution**
- TRL 8

**Dual 10Gb Ethernet**
- TRL 8

**Phased Array Antenna / Radar Interface**
- TRL 8

**PCIe Expansion**
- TRL 8

**RF Up Converter**
- TRL 8

**LO Synthesizer**
- TRL 8

**RF Down Converter**
- TRL 8

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# RARE Inter-Module I/O Bandwidths

<table>
<thead>
<tr>
<th>RARE Connector</th>
<th>Half Duplex (FPGA LVDS @ 1GHz)</th>
<th>Full Duplex</th>
<th>Bandwidth (per Connector)</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Clusters</td>
<td># of LVDS Pairs</td>
<td>LVDS Total (MB/s)</td>
<td>LVDS Total (MB/s)</td>
</tr>
<tr>
<td>X</td>
<td>3</td>
<td>7</td>
<td>21,000</td>
</tr>
<tr>
<td>Y</td>
<td>3</td>
<td>7</td>
<td>21,000</td>
</tr>
<tr>
<td>Z</td>
<td>2</td>
<td>13</td>
<td>26,000</td>
</tr>
</tbody>
</table>

## Total Bandwidth (per RARE Module)

<table>
<thead>
<tr>
<th>RARE Connector</th>
<th>Total Bandwidth (Dual Connectors per Direction)</th>
<th>Total Bandwidth per RARE Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>13.25 GB/s</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>9.25 GB/s</td>
<td>39.00 GB/s</td>
</tr>
<tr>
<td>Z</td>
<td>16.50 GB/s</td>
<td></td>
</tr>
</tbody>
</table>

RARE Modules Balance High Bandwidth Cross-Channel I/O with Processing to Maximize Performance

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Fabric Communication without Dedicated Switch Cards

- PCIe switches built into modular architecture
- End points can be FPGAs or General Purpose Processors

- FPGAs also interconnect with low latency, high bandwidth across the 3D topology
  - LVDS
  - SerDes
Integrated Health and Status Monitoring

• I²C network of microcontrollers distributed throughout architecture for health and status
  – ADCs built into microcontrollers monitor voltages, currents, and temperatures
  – Sequences power supplies and protect modules in event of supply issues or overheating
  – Microcontrollers can shut down modules or system when tolerances are not within defined limits

• Fully programmable
Software Development Kit

• Leverages open source
  – Avoids sole source proprietary operating systems
  – Lower TOC
  – Can be tailored by user

• SDK handles module communication protocols and data movement between processors and FPGAs
  – Linux kernel
  – Fedora x86-64 gcc cross compiler tool chain
  – U-Boot boot loader
  – Core root file system
Model-Based Programming

• Code wrappers encapsulate modules and enable MATLAB® / Simulink® tool flows for VHDL and C code development
  – Model desired algorithms and functionality
  – Map functions onto computing elements hosted on RARE modules
  – Define interfaces between elements
  – Generate embedded application code

• Benefits
  – Gain insight into behavior of complex algorithms
  – Eliminate need for different tool flows and skill sets
  – Quickly optimize the approach and converge on a solution
  – Model also serves as a test bench to verify implementation

Enables quick turn from algorithmic concept and simulation to implementation
## Packaging Examples

### Platform-Ready Deployment
- Fits specific platform installation envelopes
- Tight physical integration with antenna and RF subsystems

### Tailored Box-Level Solutions
- Supports variety of module counts
- System level interfaces can be brought out to panel bulkheads (digital and analog)

### Standard 19” Rack Mount Enclosure
- Supports variety of module counts based upon chassis height and depth
- System level interfaces can be brought out to panel bulkheads (digital and analog)

### Flexible Interconnections for Form Fitting SWaP
- Flexible cable-based connections
- Fully customizable cable lengths
- Increases bandwidth for stacked systems
- Right angle and straight connectors available
- Facilitates module replacement within mesh

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Example Applications

• RARE architecture is being utilized by multiple DoD agencies to meet C-SWaP within challenging installation footprints

• Two examples
  – Programmable MIMO radar transmit / receive system
  – Sense and Avoid radar for UAVs
Example 1: Multichannel DREX

- Programmable MIMO radar transmit / receive system
- Uses three COTS RARE modules
  - 2x exciter channels (1 GHz)
  - 10x receive channels (160 MSPS)
  - 3x Virtex-6 FPGAs
  - 1x PPC
  - 2x 1GbE
- Electronics: 6.25” x 6.25” x 4”
- Dual 10GbE can be supported through the addition of one more module
Example 2: Sense and Avoid Radar

- Autonomous sense and avoid capability needed in unmanned aerial systems (UAS)
- Addresses safety and compliance concerns which prevent UAS from operating freely within national airspace
- Limits ability for UAS to help with
  - Boarder patrol
  - Weather monitoring
  - Wildlife monitoring
  - Search and rescue
  - Local law enforcement
  - Disaster relief / emergency response
- UAS platforms typically very SWaP constrained
RARE: Enabling Technology for Radar
Tight Integration onto Phased Array

Antenna Sub-Assembly
Includes heat sink and mounting hardware

RF Sub-Assembly
Up converter
Down converters
LO synthesis
RF filters

approx. 21.25" x 16" x 5.5"

Digital Electronics Sub-Assembly
6 computing modules in 2 layers
(capacity = 9 in 3 layers)

Flexible RF
Up/down Convert; Master LO

Fully Programmable Digital
6 Modules in 2 Layer L-shape

Electronics Behind ESA Panel
RARE-Enabled Search/Track Radar

Tow Plane Towing Glider
Turning Away From RADAR
Towards Mountains

5 Degrees Up Beam Steer
Summary

• RARE enables high performance embedded computing in form-factor challenged installation envelopes
  – Heterogeneous
  – Scalable modularity
  – 3D connectivity

• Graphical programming methodology facilitates rapid integration and deployment

• Solutions can be made less costly and more scalable in finer-grain increments than architectures employing legacy backplanes

• Award winning technology currently being utilized in multiple DoD programs
Acknowledgements

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Thank You!

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Colorado Engineering Overview

- Company mission
  - Engineering excellence
  - Rapid response
  - Low cost
- Founded 2003
- Located in Colorado Springs, CO
- No outside investment
- Woman-owned small business (8m)
- Facility Clearance
- Winner of Tibbetts and Nunn-Perry awards
- Recognized industry leaders in MOSA applications
- 30 Phase I/II SBIR & STTR awards
- Over 37 technologies deployed in DoD and Government systems