

Reconfigurable Advanced Rapid-prototyping Environment (RARE)

A Computing Technology for Challenging Form Factors

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Abstract — The size, weight, and power (SWaP) budgets available to support embedded computing in airborne platforms, especially unmanned vehicles, are typically very constrained. Legacy backplane-centric approaches limit a designer’s flexibility to implement high performance computing in these tight spaces. This paper describes an out-of-the-box architectural approach, developed under a program sponsored by the Missile Defense Agency (MDA), enabling modular, scalable, high performance embedded computing within challenging SWaP footprints.

Keywords – modular, scalable, high performance embedded computing, heterogeneous processing

I. INTRODUCTION

An ideal high performance computing environment should encompass a variety of processing technologies so the engineer can optimize the solution to fit the size, weight, and power (SWaP) budget. General purpose / multi-core processors, Field Programmable Gate Arrays (FPGAs), graphics processors, and Application Specific Integrated Circuits (ASICs) all represent different points in the trade space of computing horsepower, power consumption, and programmability.

When implemented within a modular, scalable architecture, such heterogeneity allows the designer to choose the right computing technologies for the job and optimize the solution. However, these computing approaches have traditionally relied on backplanes which add weight, cost, and bulk to the overall system. Backplanes dictate the physical orientation and number of boards available for installation, severely limiting the designer’s ability to realize high performance, scalable computing solutions in physical volumes not conducive to legacy backplane form factors.

MDA funded an SBIR Phase I and II program to architect and develop technology addressing the challenges of modularity, scalability, and heterogeneity in deployments with challenging form factors. The program was named RARE (Reconfigurable Advanced Rapid-prototyping Environment) and executed by Colorado Engineering Inc. under the technical guidance and influence of NRL, NSWC, and ONR. This paper will describe the architecture, its benefits, and provide real-world examples of its application.

The computing technology presented in this paper was sponsored by the Missile Defense Agency under the Small Business Innovative Research (SBIR) program.

II. MODULARITY AND SCALABILITY WITH NO BACKPLANE

RARE is a modular, scalable heterogeneous processing architecture facilitating high performance embedded computing in strict cost and SWaP budgets. It provides the engineer with installation flexibility not possible with backplane-centric approaches. This award-winning technology (Fig. 1) is currently being used across multiple RF sensor designs spanning a variety of missions including ground imaging, collision avoidance, and target acquisition.

RARE defines an open-systems, “out-of-the-box” approach to embedded processing architectures by decomposing a system into functional building blocks of commercial-off-the-shelf (COTS) hardware. The blocks provide a modular way to achieve loosely coupled common operational subsystem components. Tying these components together using well-defined interfaces results in a complete, scalable high performance embedded computing system.

Processing systems targeted for platforms ranging from small UAVs to large manned aircraft can be realized using these same building blocks. RARE modules (Fig. 2) are based upon state-of-the-art general purpose processors, FPGAs, graphics processors, A/Ds, D/As, and standard I/O fabrics to facilitate high performance embedded computing system design and heterogeneous implementation within challenging installation volumes.



Figure 1. The Small Business Association presented CEI with the Tibbetts Award (left) in recognition of RARE’s innovate approach to embedded computing within challenging SWaP environments (right).

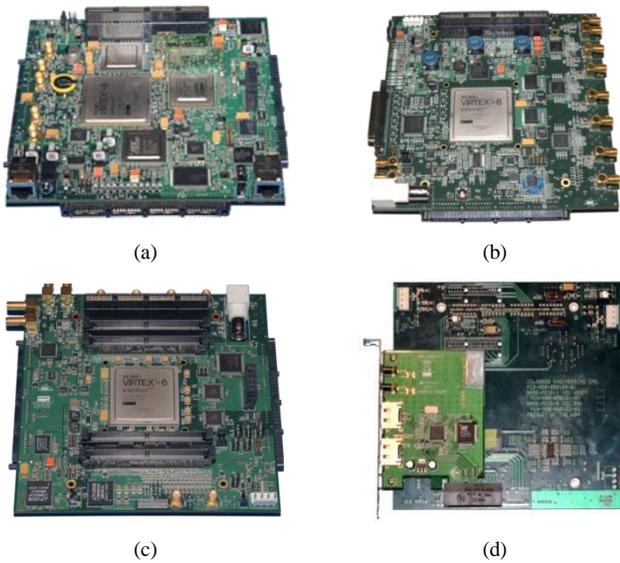


Figure 2. Example RARE modules: (a) PowerPC + Xilinx Virtex 6 FPGA; (b) 10 channel 16b/160MSPS A/D + Virtex 6 FPGA; (c) Dual channel 16b/1GSPS D/A + Virtex 6 FPGA; and (d) PCIe expansion adapter.

RARE modules are 6.25” by 6.25” cards that have multiple parallel and serial high speed interface connections in all three dimensions (Fig. 3). This allows integrators to stack and/or tile the RARE building blocks to simultaneously address processing load, I/O bandwidth, and physical installation footprint. For example, tiled structures fit well on the back of phased array antennas, while vertical stacking can realize dense processing cubes. Systems can be physically reconfigured to address different footprints while maintaining common hardware, firmware, and software across platforms and families of processing solutions. Modules can also be integrated using cable-based connections. Such approaches (Fig. 4) allow for maximum flexibility when configuring embedded processing systems for spaces where backplanes simply will not fit.

A key distinguishing feature of RARE modules is that they are stand-alone; they do not require a backplane or chassis infrastructure for connectivity. They plug together directly, thus supporting system modularity and fine-grain scalability. RARE’s ability to increase processing horsepower or channel count on a small incremental basis reduces system board count, increases reliability, and reduces total ownership cost by optimizing the amount of hardware to what is needed to achieve the system.

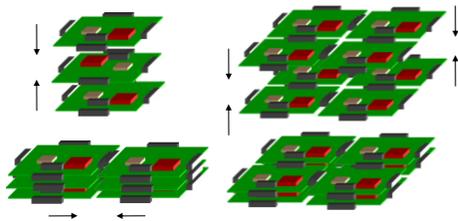


Figure 3. RARE modules connect in all three dimensions to enable embedded computing solutions in physical footprints not easily addressed by legacy backplane architectures.

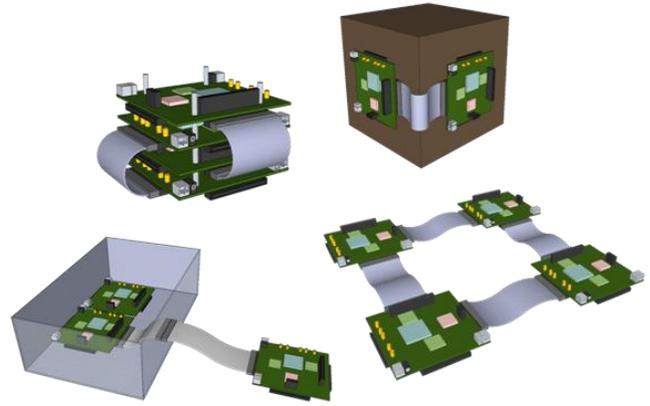


Figure 4. RARE modules connected with (optional) flexible cables can address a wide-variety of installation challenges. The addition of cables can increase the available bandwidth between modules as well as create embedded computing solutions that can “bend” to fit within tight spaces.

III. HIGH BANDWIDTH THREE DIMENSIONAL CONNECTIVITY

Multiprocessing systems must provide a balance of high bandwidth cross-channel I/O and processing to achieve performance. The RARE architecture supports high capacity PCIe, LVDS, and SerDes communication links/fabrics between processing elements leveraging the three-dimensional (3D) connectivity between modules. A single RARE module provides 39 GB/sec of bandwidth with full crossbar functionality. Processing elements can communicate over a PCIe switched serial fabric while FPGA-specific elements can simultaneously use SerDes and LVDS to build 3D interconnects (Fig. 5) for extremely low-latency applications requiring high bandwidth cross-channel communications (such as digital beamforming). Legacy backplane connectivity approaches do not generally provide for dedicated FPGA communication planes.

Backplane architectures such as VXS and VPX typically rely on dedicated switch cards to support fabric connections between processing elements. RARE’s integrated PCIe routing technology eliminates the need to spend dollars and SWaP resources on dedicated switch cards. Eliminating the need for a backplane and switch cards increases a designer’s flexibility to configure high performance embedded computing solutions in challenging installation envelopes.

RARE’s 3D connector topology also provides distributed I²C leveraging on-board microcontrollers. The network provides real-time health monitoring across the modules. The microcontrollers precisely monitor all voltages, currents, and temperatures in the system and can shut down modules if a problem is detected. The monitoring network also controls voltage sequencing and power distribution. RARE’s embedded real-time health monitoring is key to supporting the requirements of mission-critical applications.

In addition to the inter-module 3D connectivity, the RARE architecture provides “off module” interfaces including 1Gb/10Gb Ethernet, USB, JTAG, SPI, short-range wireless, and RS-232. The variety of standard interfaces supported

within the RARE family promotes network connectivity with a wide range of 3rd party systems and subsystems, including commercially available switches and routers, and promotes the net-centric integration of a system-of-systems.

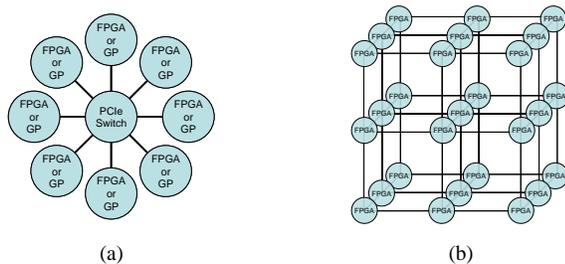


Figure 5. RARE modules enable 3D connectivity between processing elements. General purpose processors and FPGAs can be networked over PCIe (a), while FPGAs can also be directly connected in a three dimensional mesh using LVDS.

IV. GRAPHICAL PROGRAMMABILITY

In addition to developing a novel computing architecture for SWaP constrained applications, the MDA program also focused on facilitating model-based programmability. MATLAB® and Simulink® are defacto-standard tools for systems engineering, algorithm development, modeling, and simulation. RARE provides software wrappers around each module which enables their representation in a Simulink® environment. Thus, a systems engineer can map functional blocks onto the processing elements distributed across multiple RARE modules and define the I/O mechanisms between the elements (Fig. 6). The approach facilitates the transition from algorithmic concept to deployable embedded computing solutions.

Designers create models of embedded processing functions, gain insight into the behavior of complex algorithms, facilitate trade space decisions, and quickly optimize the approach. The flow allows engineers to rapidly converge on an embedded computing implementation meeting throughput, latency, and SWaP targets. It accelerates the design and verification process by eliminating the iterative, time consuming steps of converting MATLAB® and Simulink® models into C or VHDL code and generating the resulting embedded applications with separate tool flows and different engineering skill sets.

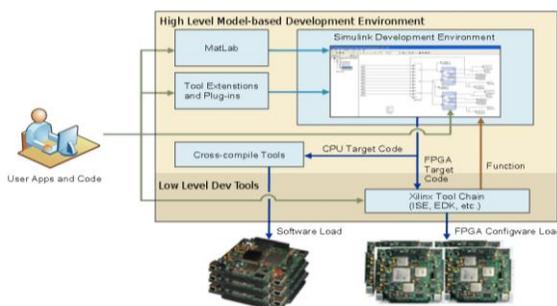


Figure 6. RARE's Simulink® tool flow enables modeling, simulation, and performance projections to facilitate transition from algorithms to solutions deployable in form-factor challenged environments.

As requirements evolve, the designer need only modify the Simulink® model to quickly regenerate the embedded firmware and/or software. The model also serves as a test bench to verify implementation; it is an executable specification that describes the larger system.

V. EXAMPLE APPLICATIONS

Multiple DoD agencies are utilizing RARE to realize high performance embedded computing in systems not easily addressed by traditional backplane centric form factors. One example is a ship-based phased array radar program focused on scalability and affordability. RARE technology enables a digital receiver which integrates into the back of the phased array and can scale from 10s to 100s of channels.

Another example is a small footprint programmable radar collection system (Fig. 7). This application takes full advantage of RARE's ability to provide high channel count and processing in a small space. The module stack up used to realize the system is 6.25" x 6.25" x 4" and contains two D/As, 10 A/Ds, three Xilinx Virtex-6 FPGAs, a PowerPC, and two 1Gb Ethernet ports for networking to other systems. In this configuration the FPGAs and PPC have PCIe connectivity while the FPGAs also communicate directly via LVDS. The operator can upload transmit waveforms, select modes, set PRFs, and enable collection windows to test radar waveforms in a real-world environment with this small footprint system.

A third example is the realization of radars supporting sense-and-avoid (SAA) systems in UAVs. SAA systems are currently being developed to allow UAVs to operate in FAA controlled airspace. Transponders can be used to help manage the paths of cooperative air traffic, but "non-cooperative" airplanes, which don't have such transponders, must also be considered. Radar is used to search and track both cooperative and non-cooperative air traffic. Target reports feed algorithms which fuse data from multiple sensors and direct the flight path of the UAV to avoid collision threats. RARE is enabling this emerging class of SAA radar solutions by providing an architecture supporting the strict cost and SWaP that UAVs demand. Digital receivers, exciters, radar signal processing, coherent clock distribution, and antenna interfacing can all be realized through RARE within aggressive size, weight, and power profiles.

One specific SAA radar is using RARE to achieve a complete pulsed-Doppler radar (antenna, RF subsystem, and processing subsystem) within a volume of approximately one cubic foot (Fig. 8). RARE's ability to integrate a high performance embedded processing subsystem on the back of the phased array makes this tight packaging possible. For this application, the RARE A/D, D/A, and processor ecosystem was enhanced with the design of up/down converter and LO synthesizer modules adhering to the same modular philosophy pioneered under the MDA program.

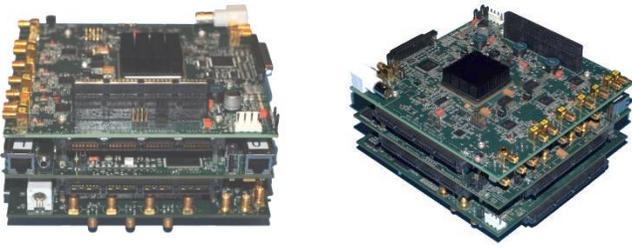


Figure 7. Different views of a three module RARE stackup supporting a multichannel digital receiver, exciter, and processor for a programmable radar collection system.

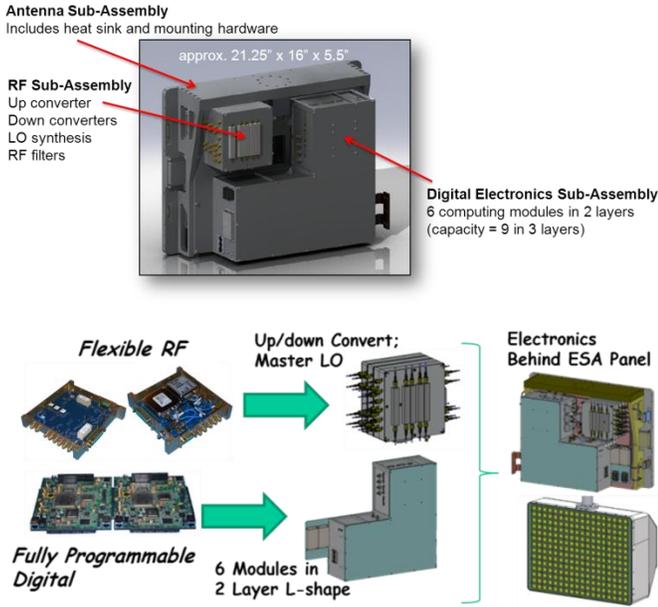


Figure 8. RARE RF and digital modules integrate onto the back of a phased array antenna to realize a pulsed-Doppler search/track radar in a volume approximately the size of a briefcase.

VI. CONCLUSION

RARE's scalable modularity, three dimensional I/O connectivity, and graphical programming methodology facilitate the rapid integration and deployment of high performance, heterogeneous, embedded computing solutions in tight SWaP envelopes. Since approaches using RARE are not constrained by backplanes, solutions can be made less costly and can be scaled in finer-grain increments for deployment in form-factor challenged installation volumes.

ACKNOWLEDGMENT

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