High Performance Embedded Computing Module
Enabled by GPU, CPU and FPGA SOCs

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Outline

• Background and Foundation
• 3D Processing
• The MPU/GPU/FPGA System on Chip (SOC) Module
  • MPU: AMD G-Series SOC (Goodbye bridges)
  • GPU: AMD E6760
  • FPGA: Altera Arria V SOC
  • PCIe mesh
• Conclusions
Background

• Ideal high performance computing environment is heterogeneous
  • Variety of processing technologies
    • General purpose / multi-core
    • Field Programmable Gate Arrays (FPGAs)
    • Graphics processors
    • Application Specific Integrated Circuits (ASICs)
  • Enables engineer to optimize solution to fit Size, Weight, and Power (SWaP) budget

• Technologies represent different points in trade space
  • Computing horsepower
  • Power consumption
  • Programmability
Background

• Heterogeneous computing approaches have traditionally relied on backplanes
  • Added weight, size, and cost
  • Constrain incremental scalability
• Backplanes limit designer’s ability to realize solutions in physical volumes not conducive to legacy form factors
• VPX isn’t VME – not as interchangeable and open
A New Approach

• MDA funded an SBIR Phase I and II program to address challenges of modularity, scalability, and heterogeneity deployments with challenging form factors
  • RARE: Reconfigurable Advanced Rapid-prototyping Environment
  • Executed by CEI under technical guidance and influence of NRL, NSWC, and ONR
  • Recipient of 2011 Tibbetts Award
  • No Backplane!

• CEI and the Navy, sponsored by MDA, defined an open approach to SWaP-friendly embedded computing architectures

• **3DR** – RARE modules connected in 3D
3DR Modularity and Scalability

- 6.25” x 6.25” cards with interface connections in 3D
  - I/O bandwidth of 39 GB/sec per module via PCIe, LVDS, and SerDes
  - 3D direct connectivity of FPGA processing elements
  - \( \text{I}^2\text{C} \) network of microcontrollers for health and status management

- Stack and/or tile modules in x, y, and z
  - Incrementally scale performance, I/O BW, and physical footprint
  - Physically reconfigure systems while maintaining common HW/FW/SW

- Solutions in a fraction of the volume of traditional backplanes
COTS Modules: Digital and RF

GP/FPGA Processor
- AMCC 460SX PowerPC
- Xilinx Virtex-6 FPGA
- Dual 1Gb Ethernet
- USB, RS-232

DAC + FPGA
- 2 DAC channels
- 16b @ 1GSPS
- Xilinx Virtex-6 FPGA

ADC + FPGA
- 10 ADC channels
- 16b @ 160 MSPS
- Xilinx Virtex-6 FPGA

Starter Kit

High Fidelity, Low Phase Noise Clock Distribution

Dual 10Gb Ethernet

PCIe Expansion

2013 Roadmap
- Stratix/Arria V
- Multicore GP
- GPU + x86 + FPGA SOCs
- Ultra-wideband ADCs
- Enhanced Tamper Resistance

RF Up Converter

Phased Array Antenna / Radar Interface

RF Down Converter

LO Synthesizer
Fabric Communication without Dedicated Switch Cards

- PCIe switches built into modular architecture (Gen 3 for new boards)
- End points can be FPGAs or General Purpose Processors

- FPGAs also interconnect with low latency, high bandwidth across the 3D topology
  - LVDS
  - SerDes
Next Generation Connectivity

Supported I/O Bandwidth by connector type for Next Generation 3DR Modules

<table>
<thead>
<tr>
<th>Connector</th>
<th>1/2 Duplex</th>
<th>Full Duplex</th>
<th>Total Bandwidth (2 connectors) (Gb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS FPGA</td>
<td>14 pairs @ 1 GHz (Gb/s)</td>
<td>PCIe Gen 3 8 Lanes @ 8 GHz (Gb/s)</td>
<td>SerDes FPGA 4 Lanes @ 6 GHz (Gb/s)</td>
</tr>
<tr>
<td>X</td>
<td>14</td>
<td>64</td>
<td>24</td>
</tr>
<tr>
<td>Y</td>
<td>14</td>
<td>64</td>
<td>24</td>
</tr>
<tr>
<td>Z</td>
<td>14</td>
<td>64</td>
<td>24</td>
</tr>
</tbody>
</table>

Flex-3DR
The GPU SoC Module
The Accelerated Processing Unit

- AMD G-Series SoC (MPU/GPU)
- North & South Bridge integrated on-chip
- Quad Core 2.0GHz MPU Cores
- 4 GB DDR3 at 1333 MHz
  - 64-bit data bus with 8-bit ECC
- Integrated Radeon 8400E GPU
  - 185 GFLOPS
- 25 W Thermal Design Power
- Gigabit Ethernet
- 75 GB NAND SATA
- 2 Mini Display Port
- USB 2.0
## The Graphics Processing Unit

<table>
<thead>
<tr>
<th>Feature</th>
<th>AMD Radeon™ E6760</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Dimensions</td>
<td>GPU + memory, 37.5 x 37.5 mm BGA</td>
</tr>
<tr>
<td>Thermal Design Power (TDP)</td>
<td>35 W</td>
</tr>
<tr>
<td>Process Technology</td>
<td>40 nm</td>
</tr>
<tr>
<td>Graphics Engine Operating Frequency (max)</td>
<td>600 MHz</td>
</tr>
<tr>
<td>CPU Interface</td>
<td>PCI Express 2.0 (x1, x2, x4, x8, x16)</td>
</tr>
<tr>
<td>Shader Processing Units</td>
<td>6 SIMD engines x 80 processing elements = 480 shaders</td>
</tr>
<tr>
<td>Floating Point Performance (single precision, peak)</td>
<td>576 GFLOPS</td>
</tr>
<tr>
<td>Display Engine</td>
<td>AMD EyeSpeed visual acceleration, AMD Eyefinity, AMD HD3D</td>
</tr>
<tr>
<td>DirectX™ Capability</td>
<td>DirectX™ 11</td>
</tr>
<tr>
<td>OpenGL</td>
<td>OpenGL 4.1</td>
</tr>
<tr>
<td>Compute</td>
<td>AMD APP, OpenCL™ 1.1, DirectCompute 11</td>
</tr>
<tr>
<td>Internal Thermal Sensor</td>
<td>Yes</td>
</tr>
<tr>
<td>Memory</td>
<td></td>
</tr>
<tr>
<td>Operating Frequency (max)</td>
<td>800 MHz / 3.2 Gbps</td>
</tr>
<tr>
<td>Configuration Type</td>
<td>128-bit wide, 1 GB, GDDR5</td>
</tr>
</tbody>
</table>
The FPGA with ARM Cores

- Altera Arria V with 2 integrated 800 MHz ARM Cortex-A9s
- 28 nm – low power

Hard processor System (HPS) Block Diagram

- 1600 GMACs
- 300 GFLOPs
- 125 Gbps between FPGA & HPS
## Arria V SoC

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Internal Memory</td>
<td>22.8 Mb</td>
</tr>
<tr>
<td>FPGA Logic Elements (LEs)</td>
<td>462,000</td>
</tr>
<tr>
<td>FPGA 18x18 Multipliers</td>
<td>2,136</td>
</tr>
<tr>
<td>FPGA 6.25 Gbps Transceivers</td>
<td>30</td>
</tr>
<tr>
<td>2 Hard PCIe Controllers</td>
<td>2 PCIe Gen3 x4 links</td>
</tr>
<tr>
<td>SERDES x4</td>
<td>SERDES x4 to 5 of 6 edge connectors</td>
</tr>
<tr>
<td>True LVDS</td>
<td>2 LVDS-7 to all 6 edge connectors</td>
</tr>
<tr>
<td>GMACS</td>
<td>1600 (FPGA + ARM Core)</td>
</tr>
<tr>
<td>GFLOPS</td>
<td>300 (FPGA + ARM Core)</td>
</tr>
<tr>
<td>Aggregate Bandwidth between ARM Core and FPGA</td>
<td>125 Gbps</td>
</tr>
<tr>
<td>ARM Core Off-board Peripherals</td>
<td>Gigabit Ethernet, UART-to-USB</td>
</tr>
<tr>
<td>ARM Cortex-9 Dual-Core Speed</td>
<td>800 MHz</td>
</tr>
<tr>
<td>FPGA Hard DDR3 Controller</td>
<td>256 MB DDR3</td>
</tr>
<tr>
<td>ARM Core Hard DDR3 Controller</td>
<td>256 MB DDR3</td>
</tr>
</tbody>
</table>
• APU is root-complex only

• Need to have one port configured to be Non-Transparent (NT)
  • During Enumeration, both APUs will treat the NT port as an endpoint from their domain
  • Address Translation Registers must be configured so that each Root Complex can access the PCIe memory address of the other domain

• Only one root complex will push/pull data to/from its domain
• CPU on Processor Board can be configured as an endpoint master
  • Eliminates the need for NT port… makes software a little more challenging
• Legacy CEI boards have 2 PCIe planes: Processor & FPGA
• PEX8780 can be configured as 2, 3, or 4 “virtual switches”
  • Each virtual switch is essentially an independent switch inside the PEX8780
  • 2 virtual switches creates 2 PCIe planes for backward X,Y,Z connectors supports 2 PCIe Gen3 x4 links or 1 PCIe Gen3 x8 link
Tying It All Together

• Heterogeneous compute platform on a single 6.25 in² PCB with connectors on all 6 sides
• AMD G-Series 4 MPU+GPU cores
• AMD E6760 GPU (576 GFLOPS)
• Altera Arria V w/ dual ARM Cortex-A9s
• PLX PCIe switch
• Provides tremendous flexibility to engineer at reasonable price for SWaP constrained applications
• Need more horsepower? Add more modules?
• Attach an ADC and DAC card for sensor processing
• Available Q1 2014
• Considering interface card for 2 MXM GPU modules
Thank You!

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