Reconfigurable Advanced Rapid-prototyping Environment (RARE):

A Computing Technology for Challenging Form Factors

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Outline

- Background
- Overview of RARE Architecture
  - Approach
  - Features
  - Software and Programming Model
  - Packaging
- Application Examples
- Summary

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Background

- Ideal high performance computing environment is heterogeneous
  - Variety of processing technologies
    - General purpose / multi-core
    - Field Programmable Gate Arrays (FPGAs)
    - Graphics processors
    - Application Specific Integrated Circuits (ASICs)
  - Enables engineer to optimize solution to fit Size, Weight, and Power (SWaP) budget
- Technologies represent different points in trade space
  - Computing horsepower
  - Power consumption
  - Programmability

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Background

- Heterogeneous computing approaches have traditionally relied on backplanes
  - Added weight, size, and cost
  - Constrain incremental scalability
- Backplanes limit designer's ability to realize solutions in physical volumes not conducive to legacy form factors

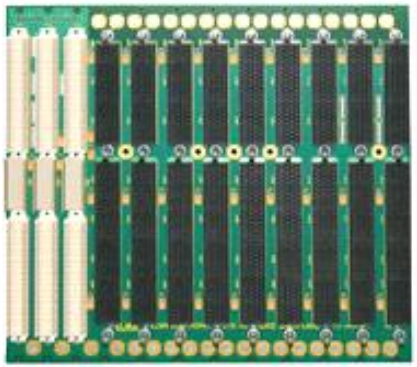

Image courtesy of Elma Bustronic

Image courtesy of Kontron

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A New Approach

- MDA funded an SBIR Phase I and II program to address challenges of modularity, scalability, and heterogeneity in deployments with challenging form factors
  - RARE: Reconfigurable Advanced Rapid-prototyping Environment
  - Executed by CEI under technical guidance and influence of NRL, NSWC, and ONR
  - Recipient of 2011 Tibbetts Award
  - No Backplane!

- Presentation will describe architecture and provide real-world application examples

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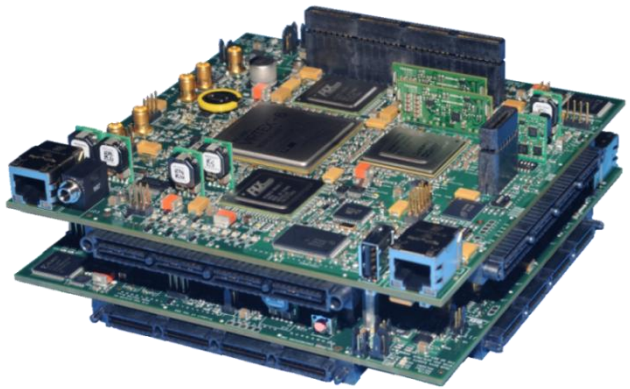
MOSA Inspired Technology

- Decomposes a system into functional COTS building blocks
- Blocks provide a modular way to achieve loosely coupled common operational subsystem components
- When tied together using well defined interfaces, blocks form a complete, scalable processing and control system



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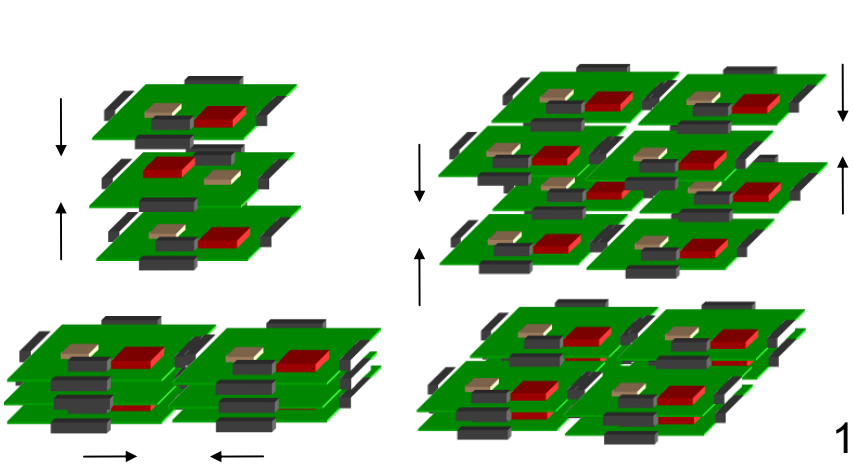
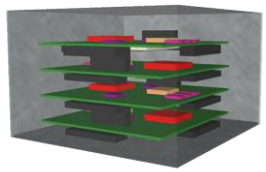
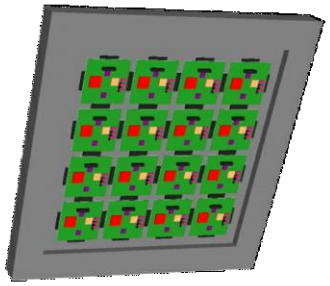
RARE Modularity and Scalability

- 6.25” x 6.25” cards with interface connections in three dimensions
  - I/O bandwidth of 39 GB/sec per module via PCIe, LVDS, and SerDes
  - 3D direct connectivity of FPGA processing elements
  - I^2C network of microcontrollers for health and status management
- Stack and/or tile modules in x, y, and z
  - Incrementally scale performance, I/O bandwidth, and physical footprint
  - Physically reconfigure systems while maintaining common HW/FW/SW
  - Solutions in a fraction of the volume of traditional backplanes

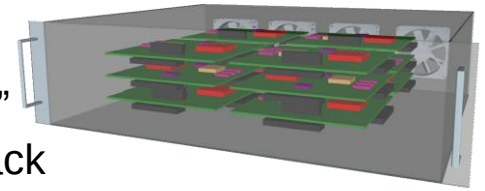




Cube



Tiled



19” Rack

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COTS Modules: Digital and RF

TRLs as of 4/5/12

GP/FPGA Processor TRL 8

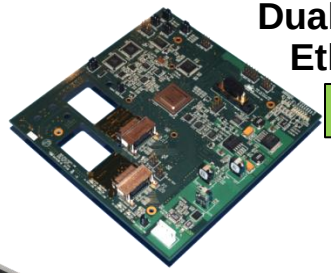
- AMCC 460SX PowerPC
- Xilinx Virtex-6 FPGA
- Dual 1Gb Ethernet
- USB, RS-232

ADC+Processor TRL 8

- 10 ADC channels
- 16b @ 160MSPS
- Xilinx Virtex-6 FPGA

DAC+Processor TRL 8

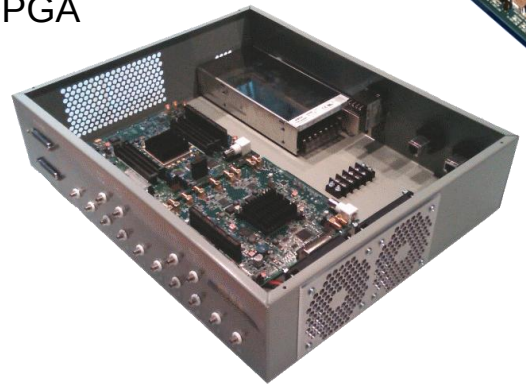
- 2 DAC channels
- 16b @ 1GSPS
- Xilinx Virtex-6 FPGA



Dual 10Gb Ethernet TRL 8

Phased Array Antenna / Radar Interface TRL 8

Starter Kit



High Fidelity, Low Phase Noise Clock Distribution TRL 8

RF Up Converter TRL 8

LO Synthesizer TRL 8

PCIe Expansion TRL 8

Roadmap

- Stratix V
- Multicore GP
- GPU + x86
- Ultra-wideband ADCs
- Enhanced Tamper Resistance

RF Down Converter TRL 8

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RARE Inter-Module I/O Bandwidths

RARE Connector	Half Duplex (FPGA LVDS @ 1GHz)				Full Duplex			Bandwidth (per Connector)
	# of Clusters	# of LVDS Pairs	LVDS Total (Mb/s)	LVDS Total (MB/s)	PCIe FPGA (MB/s)	PCIe PPC (MB/s)	SerDes FPGA (MB/s)	
X	3	7	21,000	2,625	2,000	2,000	0	6.625 GB/s
Y	3	7	21,000	2,625	0	2,000	0	4.625 GB/s
Z	2	13	26,000	3,250	2,000	2,000	1,000	8.250 GB/s

RARE Connector	Total Bandwidth (Dual Connectors per Direction)	Total Bandwidth per RARE Module
X	**13.25 GB/s**	**39.00 GB/s**
Y	**9.25 GB/s**	
Z	**16.50 GB/s**	

RARE Modules Balance High Bandwidth Cross-Channel I/O with Processing to Maximize Performance

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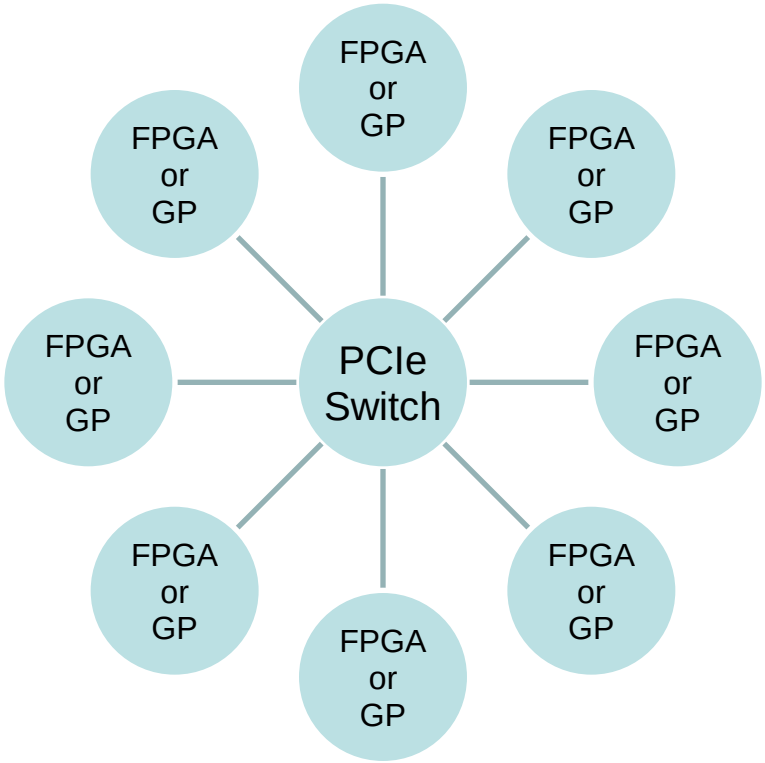
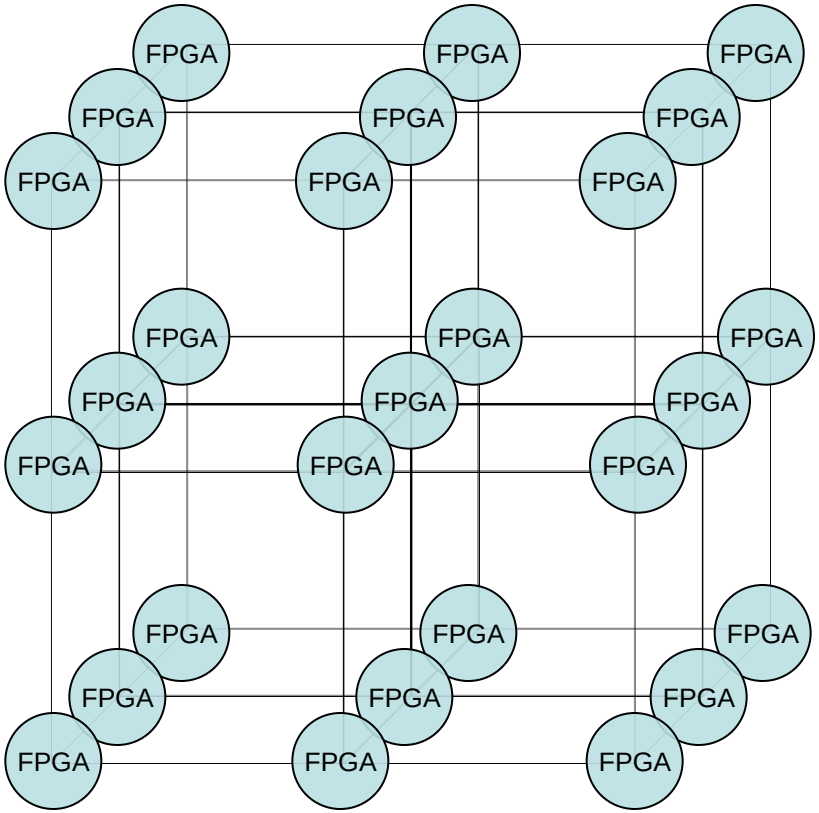
Fabric Communication without Dedicated Switch Cards



- PCIe switches built into modular architecture
- End points can be FPGAs or General Purpose Processors

- FPGAs also interconnect with low latency, high bandwidth across the 3D topology
  - LVDS
  - SerDes



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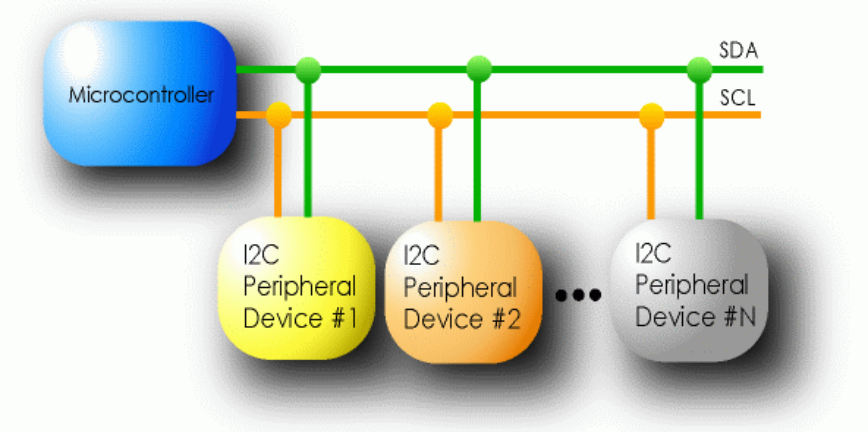
Integrated Health and Status Monitoring

- I^2C network of microcontrollers distributed throughout architecture for health and status
  - ADCs built into microcontrollers monitor voltages, currents, and temperatures
  - Sequences power supplies and protect modules in event of supply issues or overheating
  - Microcontrollers can shut down modules or system when tolerances are not within defined limits
- Fully programmable



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Software Development Kit

- Leverages open source
  - Avoids sole source proprietary operating systems
  - Lower TOC
  - Can be tailored by user
- SDK handles module communication protocols and data movement between processors and FPGAs
  - Linux kernel
  - Fedora x86-64 gcc cross compiler tool chain
  - U-Boot boot loader
  - Core root file system

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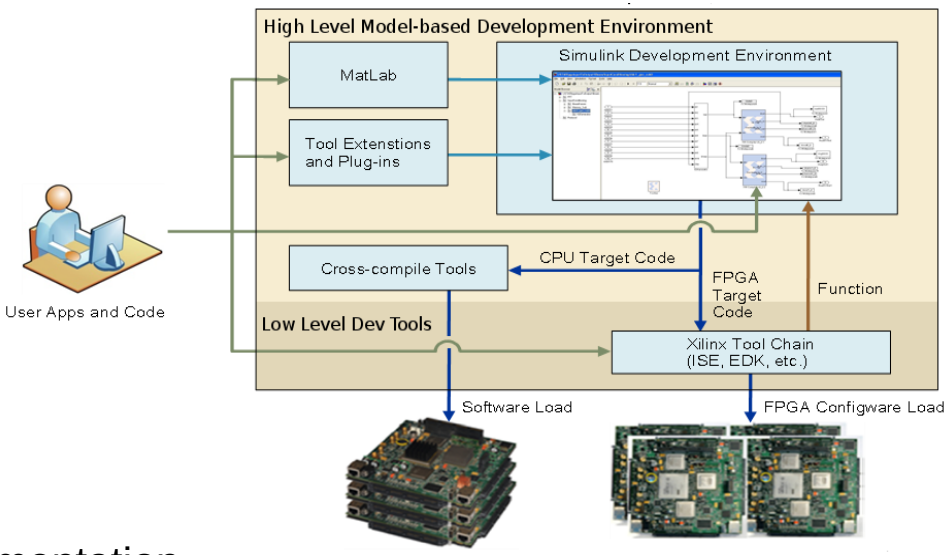
Model-Based Programming

- Code wrappers encapsulate modules and enable MATLAB® / Simulink® tool flows for VHDL and C code development
  - Model desired algorithms and functionality
  - Map functions onto computing elements hosted on RARE modules
  - Define interfaces between elements
  - Generate embedded application code
- Benefits
  - Gain insight into behavior of complex algorithms
  - Eliminate need for different tool flows and skill sets
  - Quickly optimize the approach and converge on a solution
  - Model also serves as a test bench to verify implementation



Enables quick turn from algorithmic concept and simulation to implementation

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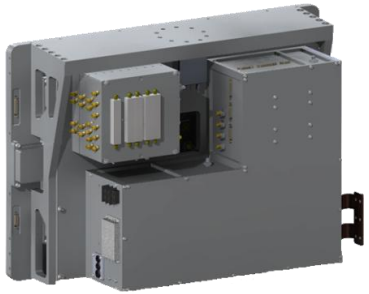
Packaging Examples

Platform-Ready Deployment

- Fits specific platform installation envelopes
- Tight physical integration with antenna and RF subsystems



Tailored Box-Level Solutions

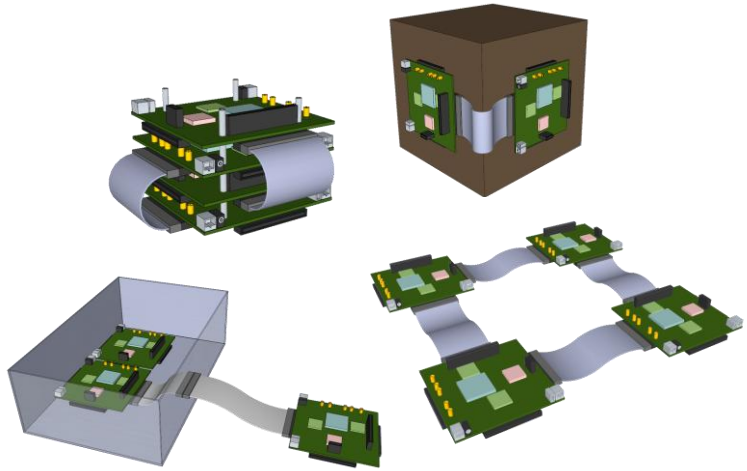
- Supports variety of module counts
- System level interfaces can be brought out to panel bulkheads (digital and analog)

Standard 19” Rack Mount Enclosure

- Supports variety of module counts based upon chassis height and depth
- System level interfaces can be brought out to panel bulkheads (digital and analog)

Flexible Interconnections for Form Fitting SWaP

- Flexible cable-based connections
- Fully customizable cable lengths
- Increases bandwidth for stacked systems
- Right angle and straight connectors available
- Facilitates module replacement within mesh



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Example Applications

- RARE architecture is being utilized by multiple DoD agencies to meet C-SWaP within challenging installation footprints
- Two examples
  - Programmable MIMO radar transmit / receive system
  - Sense and Avoid radar for UAVs

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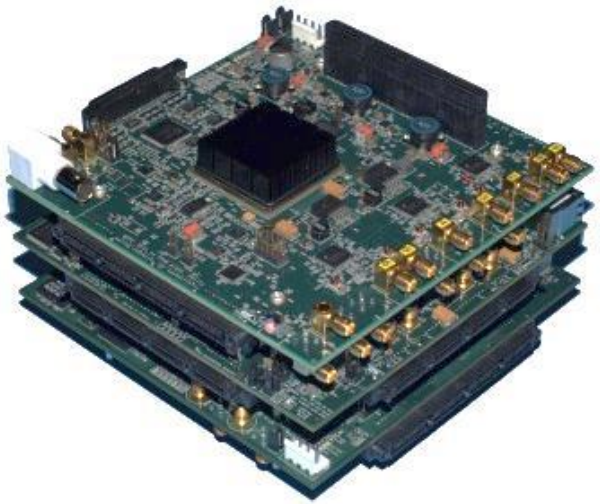
Example 1: Multichannel DREX

- Programmable MIMO radar transmit / receive system
- Uses three COTS RARE modules
  - 2x exciter channels (1 GHz)
  - 10x receive channels (160 MSPS)
  - 3x Virtex-6 FPGAs
  - 1x PPC
  - 2x 1GbE
- Electronics: 6.25” x 6.25” x 4”
- Dual 10GbE can be supported through the addition of one more module



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Example 2: Sense and Avoid Radar

- Autonomous sense and avoid capability needed in unmanned aerial systems (UAS)
- Addresses safety and compliance concerns which prevent UAS from operating freely within national airspace
- Limits ability for UAS to help with
  - Boarder patrol
  - Weather monitoring
  - Wildlife monitoring
  - Search and rescue
  - Local law enforcement
  - Disaster relief / emergency response
- UAS platforms typically very SWaP constrained

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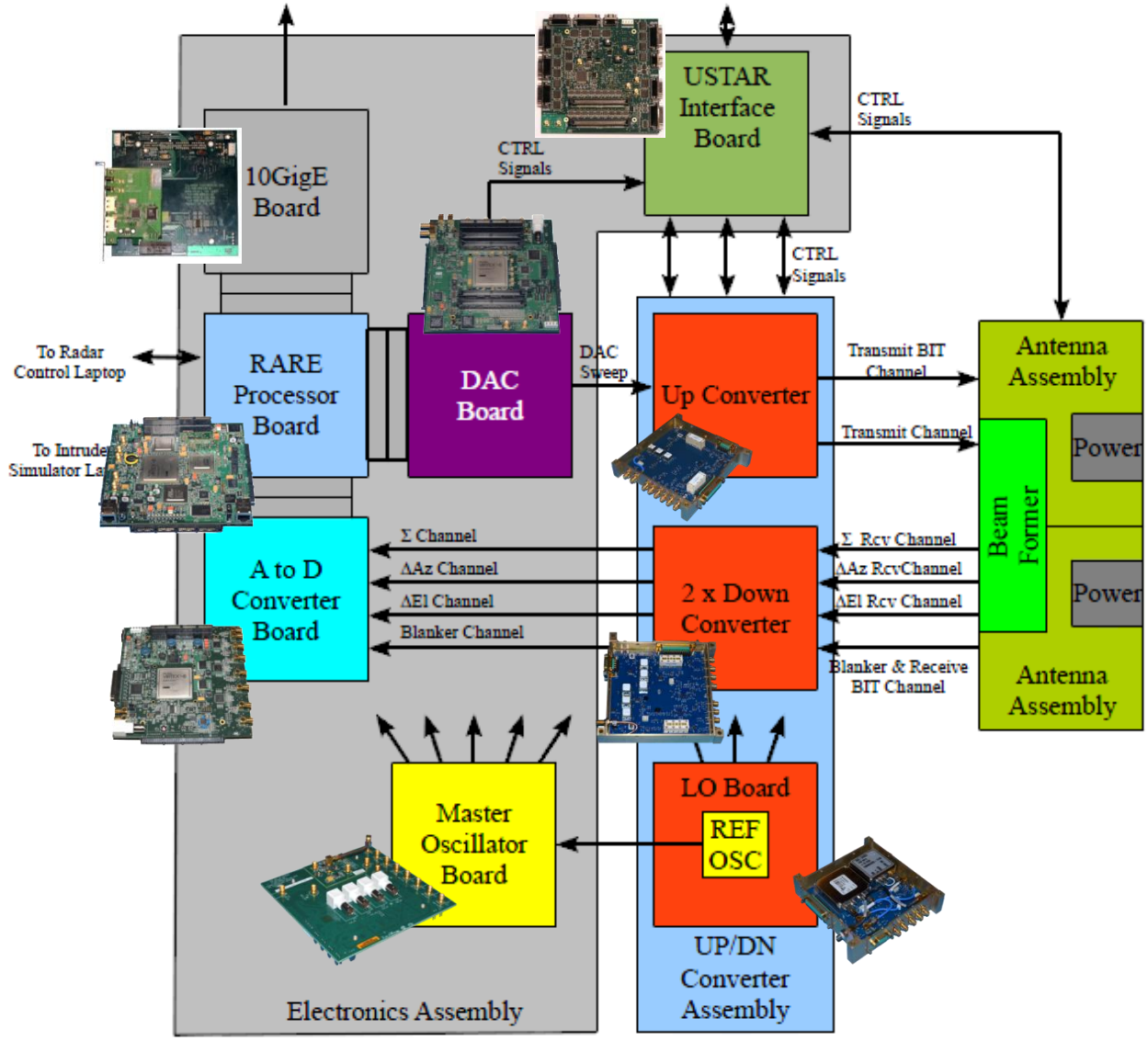
RARE: Enabling Technology for Radar



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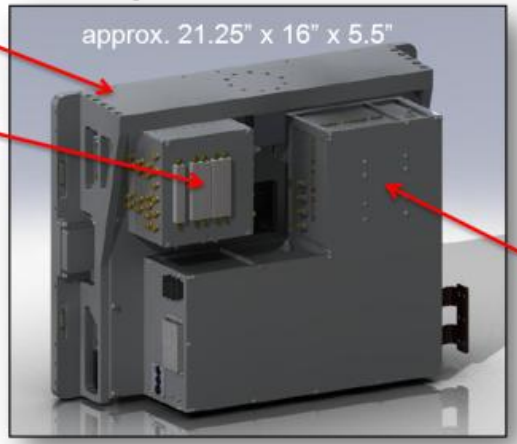
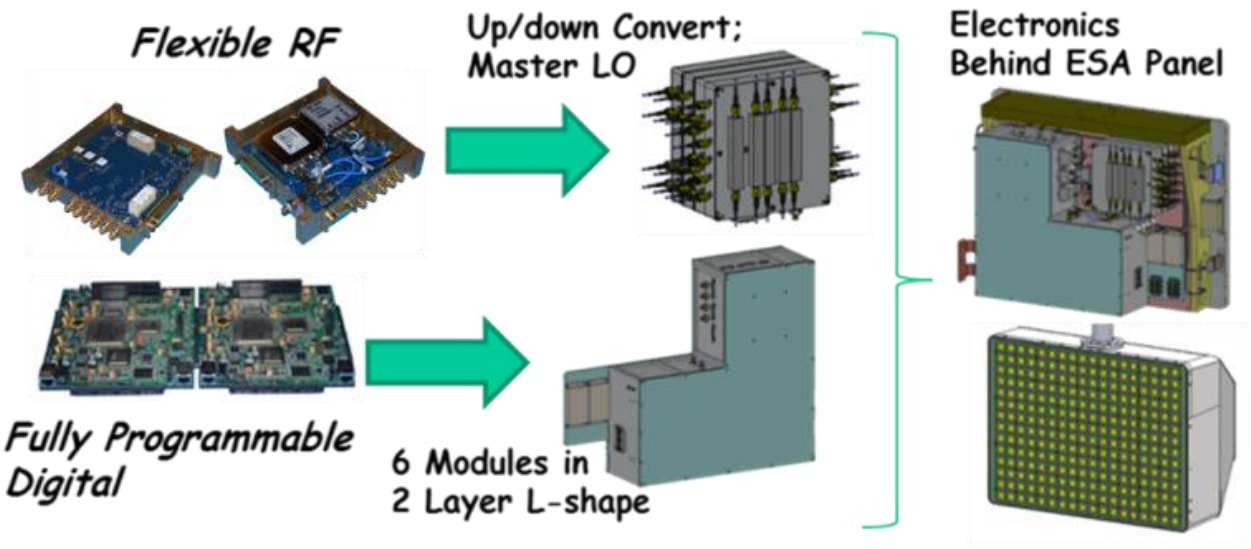
Tight Integration onto Phased Array

Antenna Sub-Assembly
Includes heat sink and mounting hardware

RF Sub-Assembly
Up converter
Down converters
LO synthesis
RF filters



Digital Electronics Sub-Assembly
6 computing modules in 2 layers
(capacity = 9 in 3 layers)



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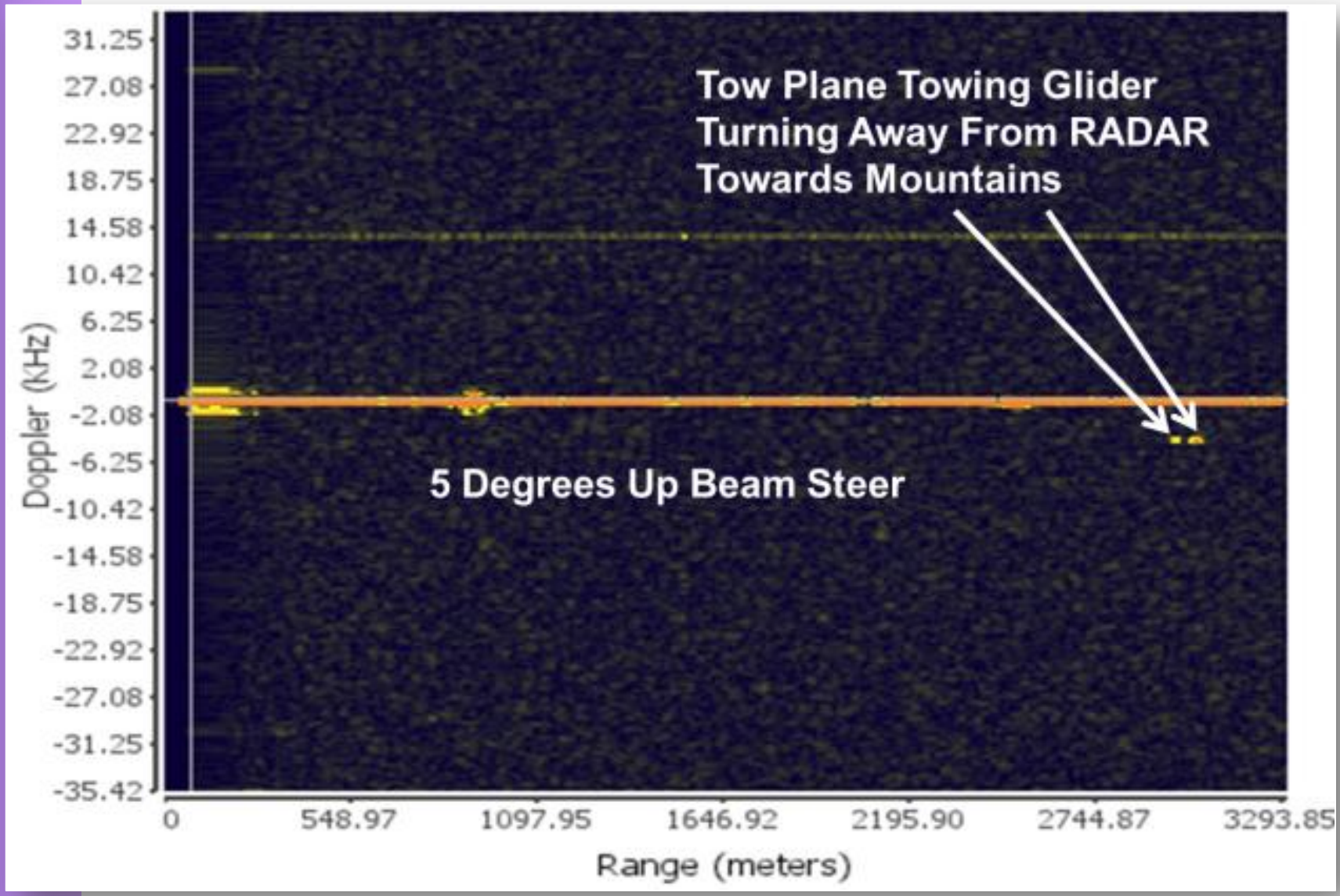
RARE-Enabled Search/Track Radar



Summary

- RARE enables high performance embedded computing in form-factor challenged installation envelopes
  - Heterogeneous
  - Scalable modularity
  - 3D connectivity
- Graphical programming methodology facilitates rapid integration and deployment
- Solutions can be made less costly and more scalable in finer-grain increments than architectures employing legacy backplanes
- Award winning technology currently being utilized in multiple DoD programs

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Acknowledgements

CEI would like to thank MDA, NRL, ONR, and NSWC for their support and guidance of the RARE SBIR Phase I and II development program

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Thank You!

For more information please contact:

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Colorado Engineering Overview

- Company mission
  - Engineering excellence
  - Rapid response
  - Low cost
- Founded 2003
- Located in Colorado Springs, CO
- No outside investment
- Woman-owed small business (8m)
- Facility Clearance
- Winner of Tibbetts and Nunn-Perry awards
- Recognized industry leaders in MOSA applications
- 30 Phase I/II SBIR & STTR awards
- Over 37 technologies deployed in DoD and Government systems