Synthetic Aperture Radar on Low Power Multi-Core DSP

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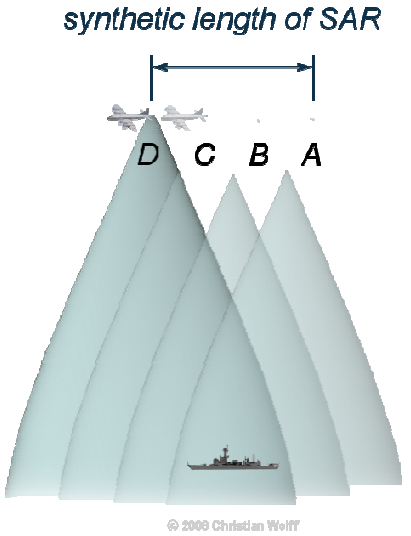
Outlines

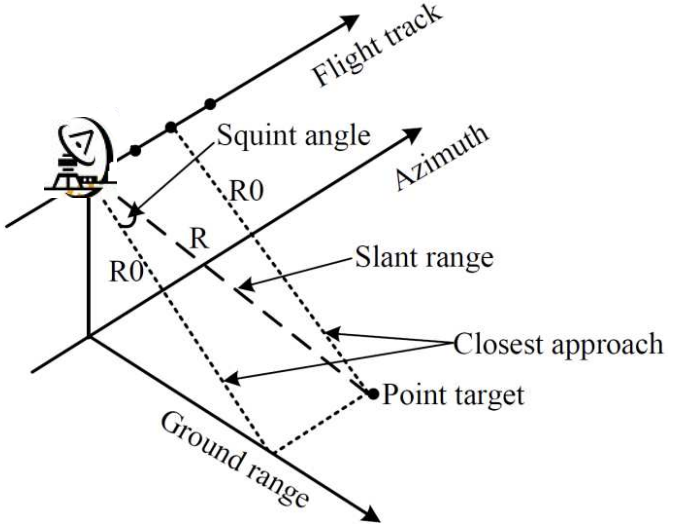
- Basics of Synthetic Aperture Radar (SAR)
- *TMS320C6678* Architecture
- SAR System Implementation on DSP
  - Modulization
  - Data flow
- Implementation Profiling
  - Module profiling
  - Single core vs. multi-core
  - Comparison with alternative platforms in literature: GPU, FPGA
- Conclusion

SAR Geometry

- Use one antenna in time-multiplex
- Use Doppler shift to obtain fine azimuth resolution
- Two dimensions
  - Range (cross-track, fast time)
    - Line-of-sight distance from radar to target
  - Azimuth (along-track, slow time)
    - Parallel to radar motion track



http://www.radartutorial.eu/20.airborne/ab07.en.html



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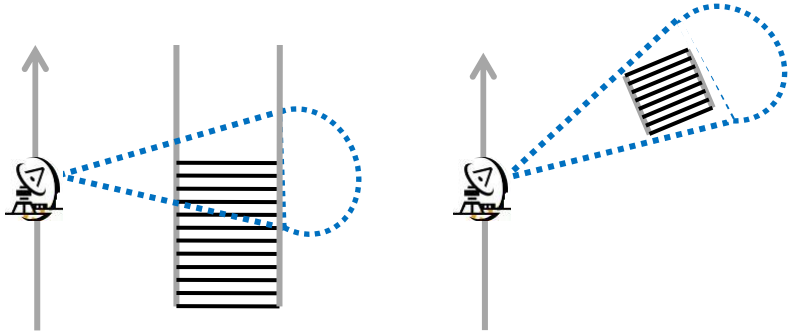
SAR Algorithm

- SAR types
  - Airborne or spaceborne
  - Strip SAR, spot SAR, etc.
  - Platforms: CPU, GPU, FPGA, etc



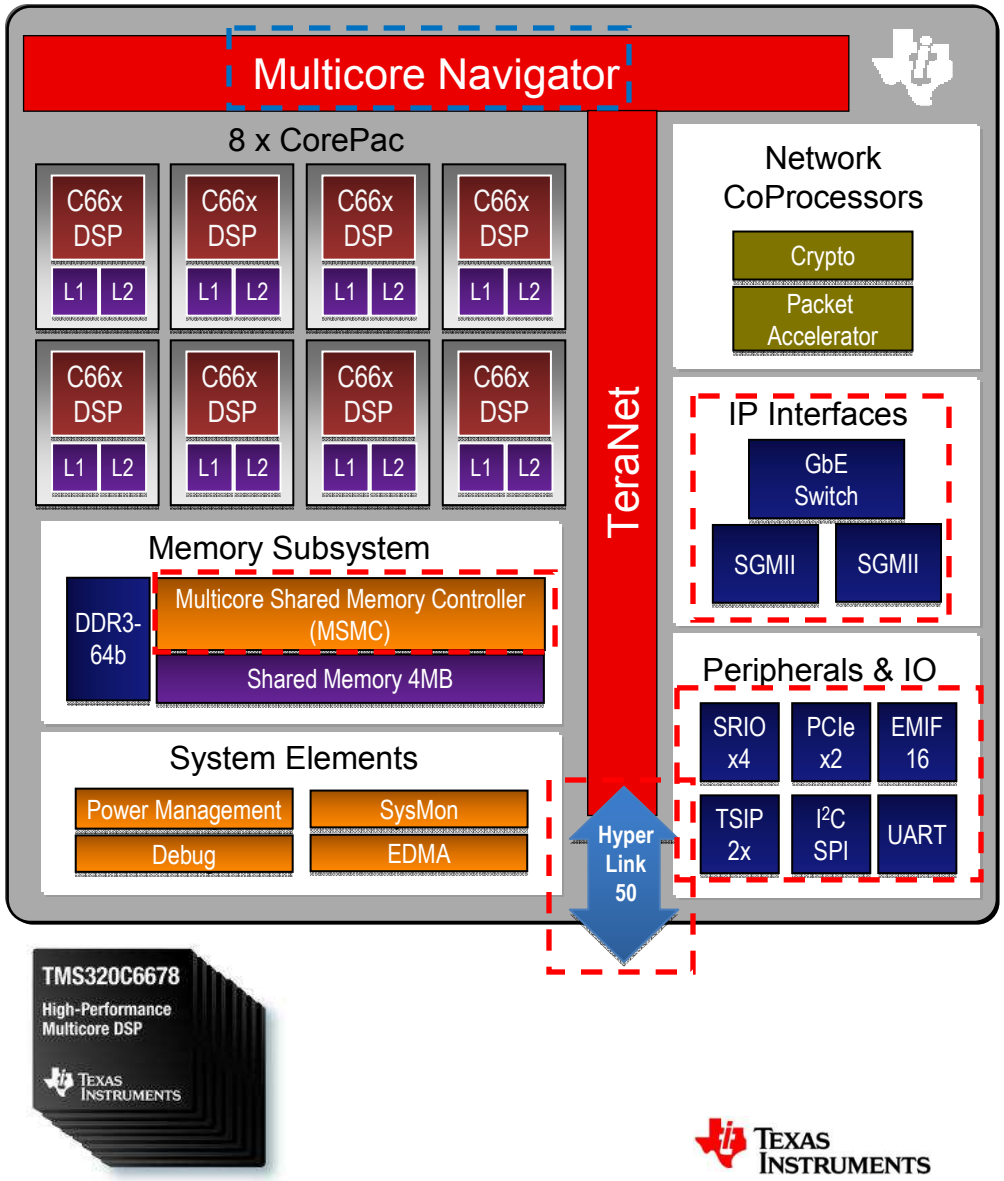
Strip mapping

Spot mapping

- Diverse algorithms
  - Range-azimuth algorithm
  - Chirp-scaling algorithm
  - Ω-k algorithm
- Range-azimuth algorithm
  - Achieve block processing efficiency
  - Separability of processing in two directions
  - Limited for low squint case

Multicore DSP (TMS320C6678): Functional Diagram

- Multicore KeyStone architecture SoC
- Fixed/Floating corePac
  - 8 CorePac @ 1.25 GHz
  - 4.0 MB Shared L2
  - Performance: 320GMAC, 160GFLOPs, 60GDFLOPs
  - Power ~10W@1GHz
- Navigator
  - Queue Manager, Packet DMA
- Multicore shared memory controller
  - Low latency, high bandwidth memory access
- 3-port GigE switch (Layer 2)
- PCIe gen-2, 2-lanes
- SRIO gen-2, 4-lanes
- HyperLink
  - Support connection to other keystone devices providing resource scalability
  - Provide a 50Gbps chip-level interconnect



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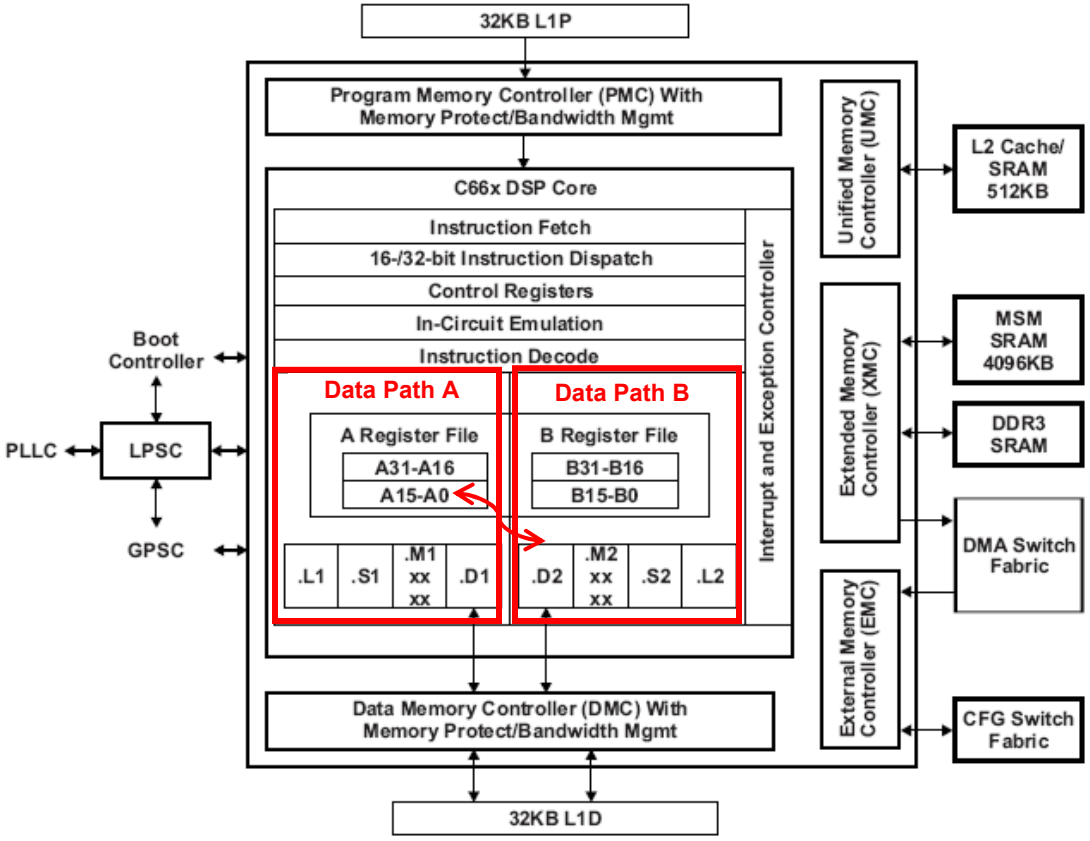
C66x – Core Architecture

- VLIW architecture
  - Can issue 8 instructions per cycle
- 2 data paths
  - 4 units per data path
  - L, S, D, M
  - Access cross data path
- 64 registers (32 bit)
  - 32 per data path
  - Can be arranged in dual (64 b or quad (128 bit) registers
- Single Instruction Multiple Data (SIMD)
  - Dual or quad multiplies (64 or 128 bits)



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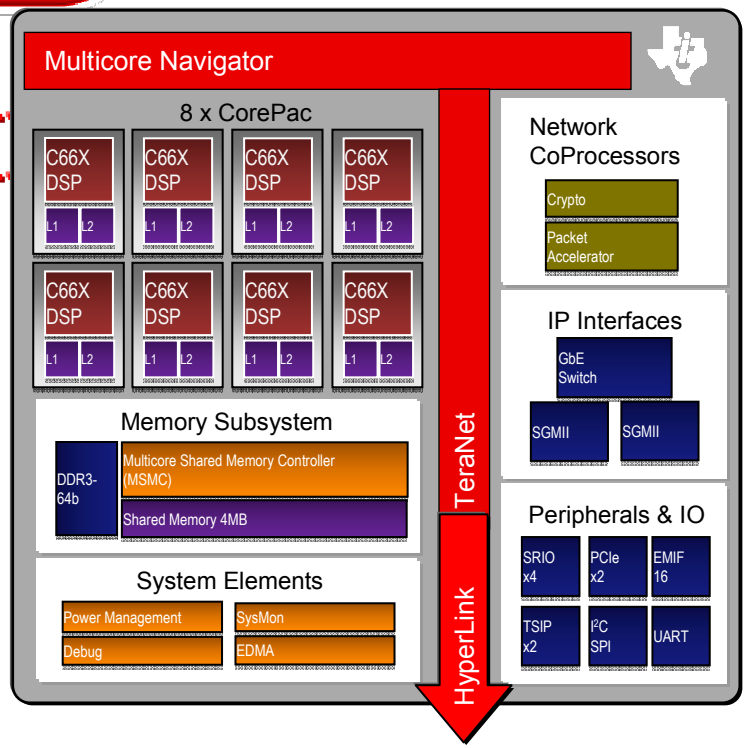
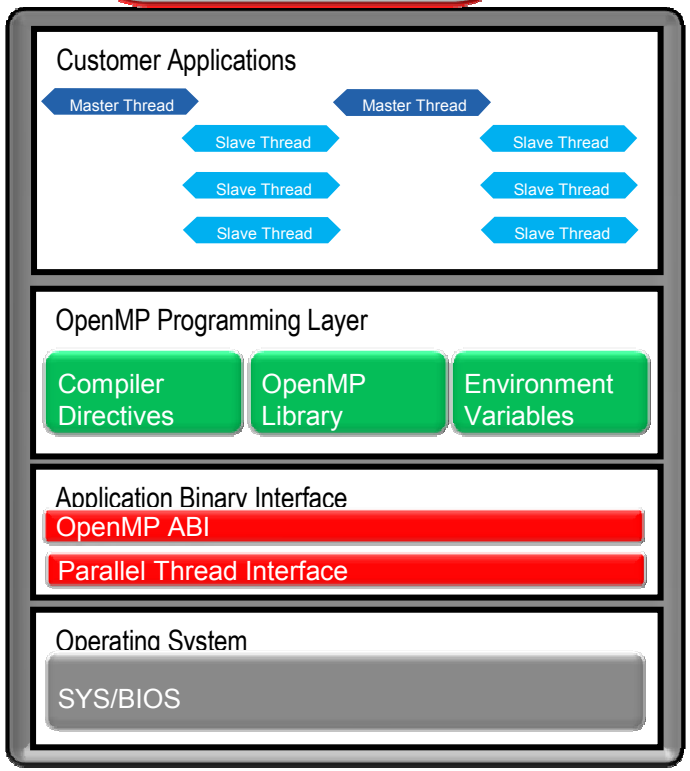
Multicore Performance Single Core Simplicity

Develop

- Code Composer Studio
- Code Generation Tools
  - Compiler, Linker
- Programming Model
  - MCSDK, OpenMP, OpenCL

MCSDK
OpenMP
OpenCL





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- 1 c6678
- 160 Gflops
- 1GByte DDR3
- 10W

- 4 c6678
- 512 Gflops
- 4GByte DDR3
- 54W

- 8 c6678
- >1 Teraflop
- 16 GByte DDR3
- 110 W

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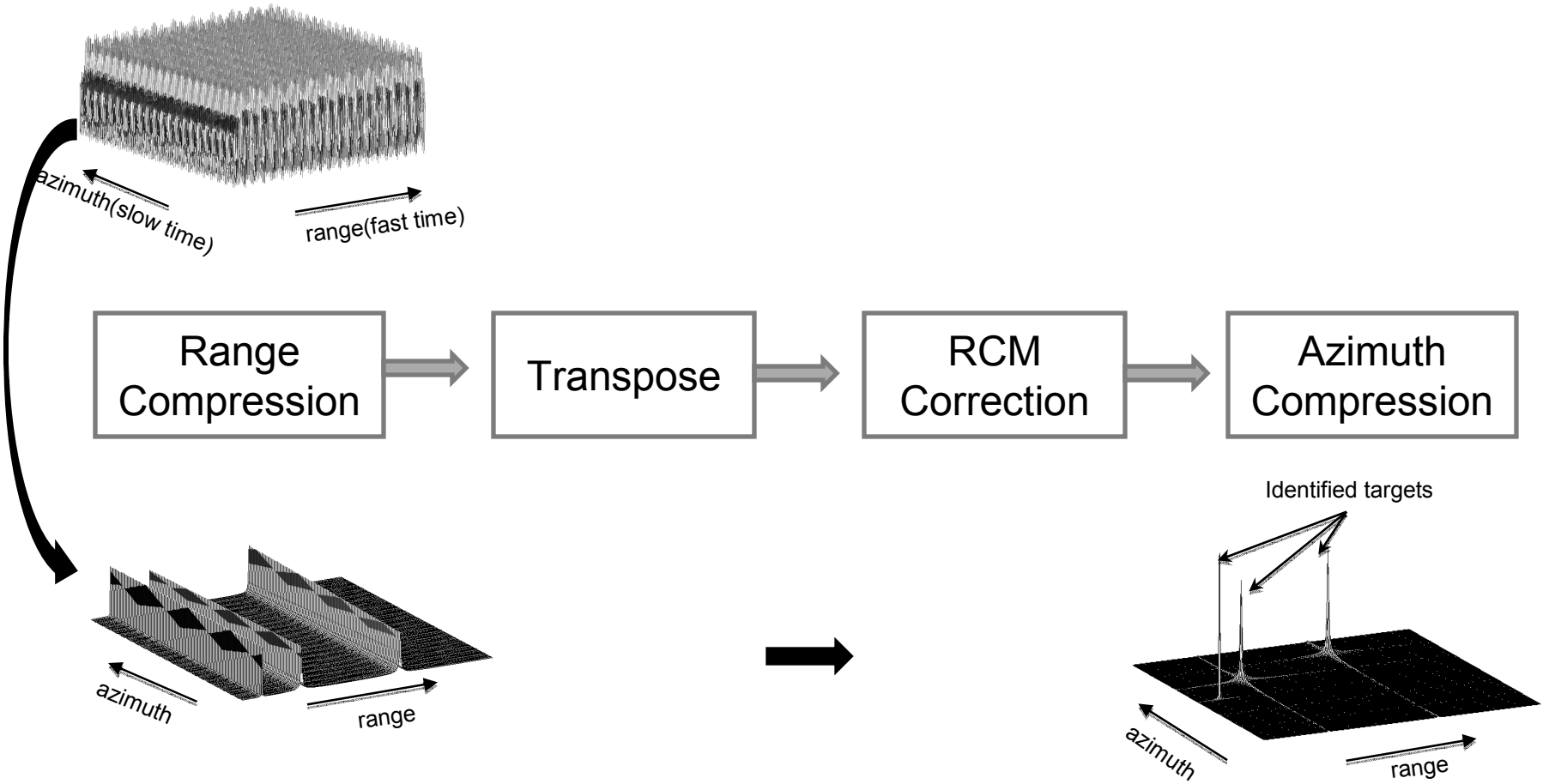
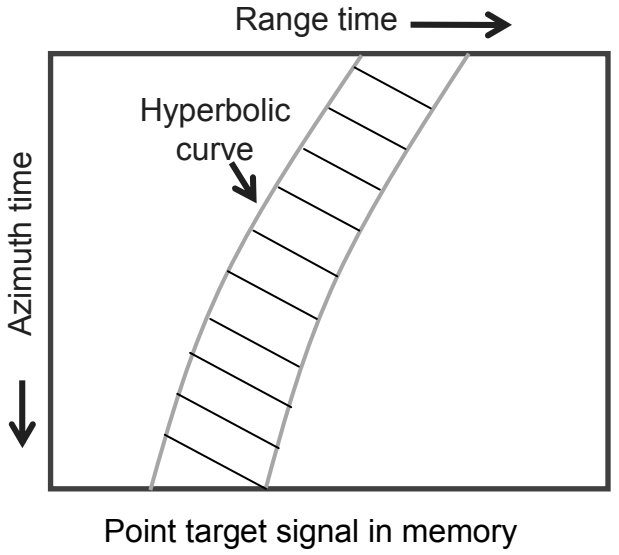
Range-azimuth Algorithm

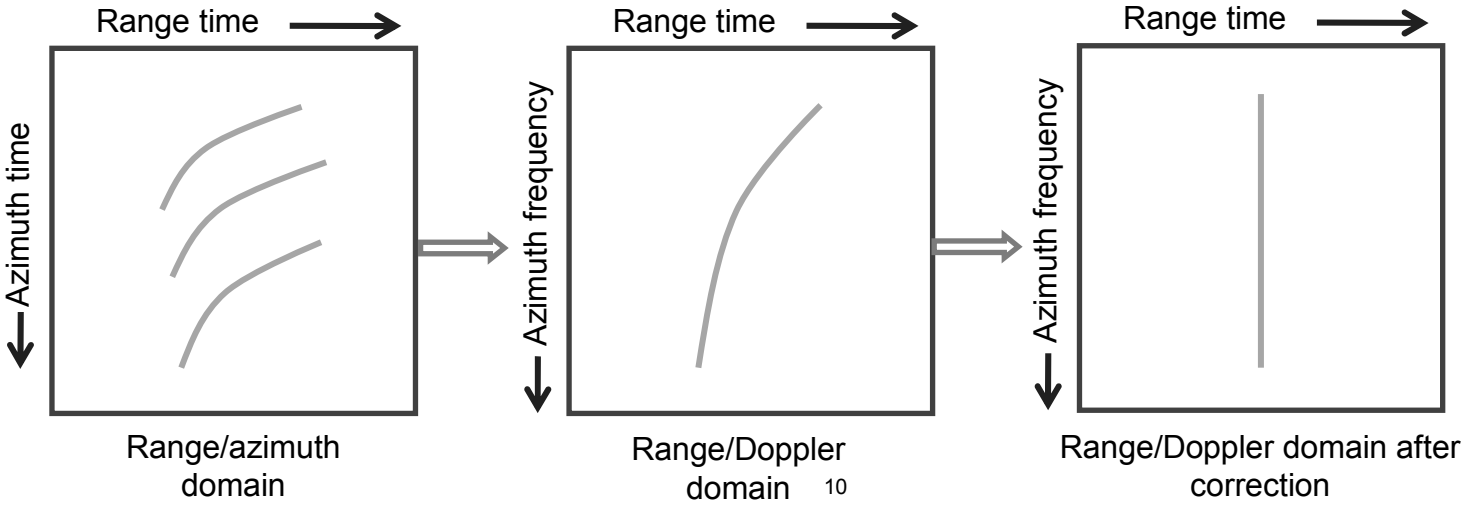
- Main steps



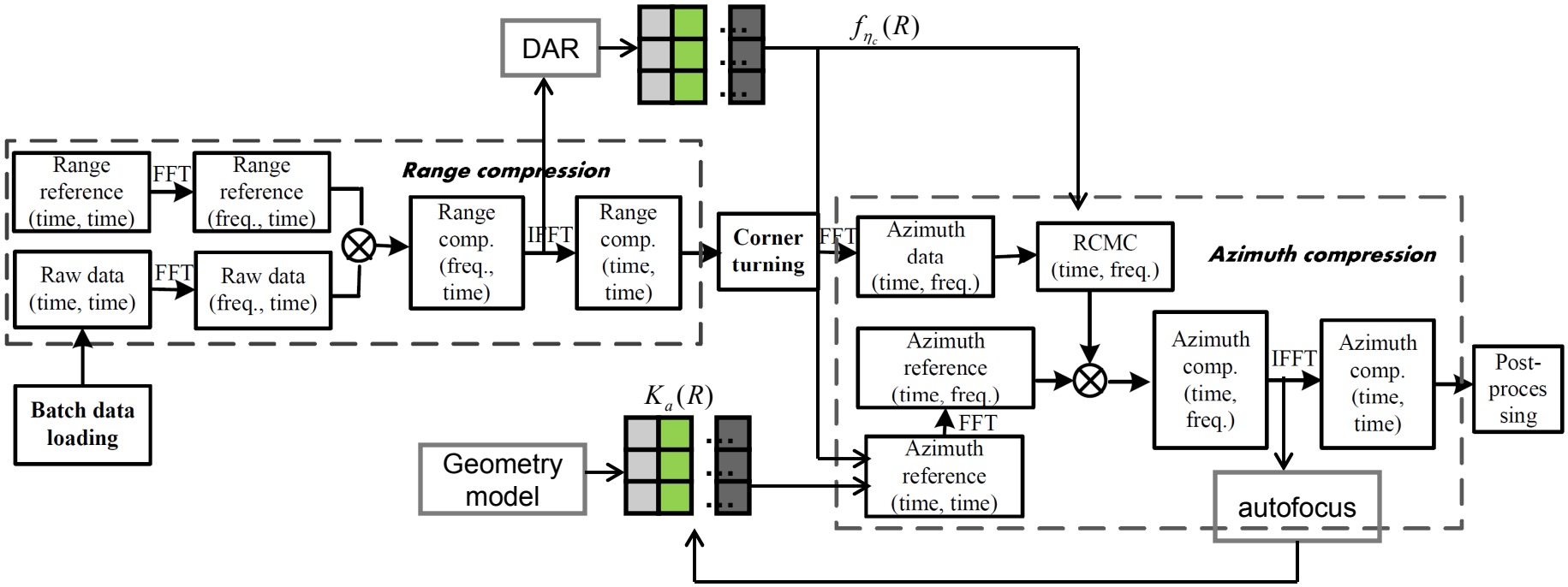
RCM Correction

- Cause
  - Instantaneous range change leads to variation in the range delay that could be larger than a range sample space
- Range-Doppler correction
  - Interpolation in range-Doppler domain

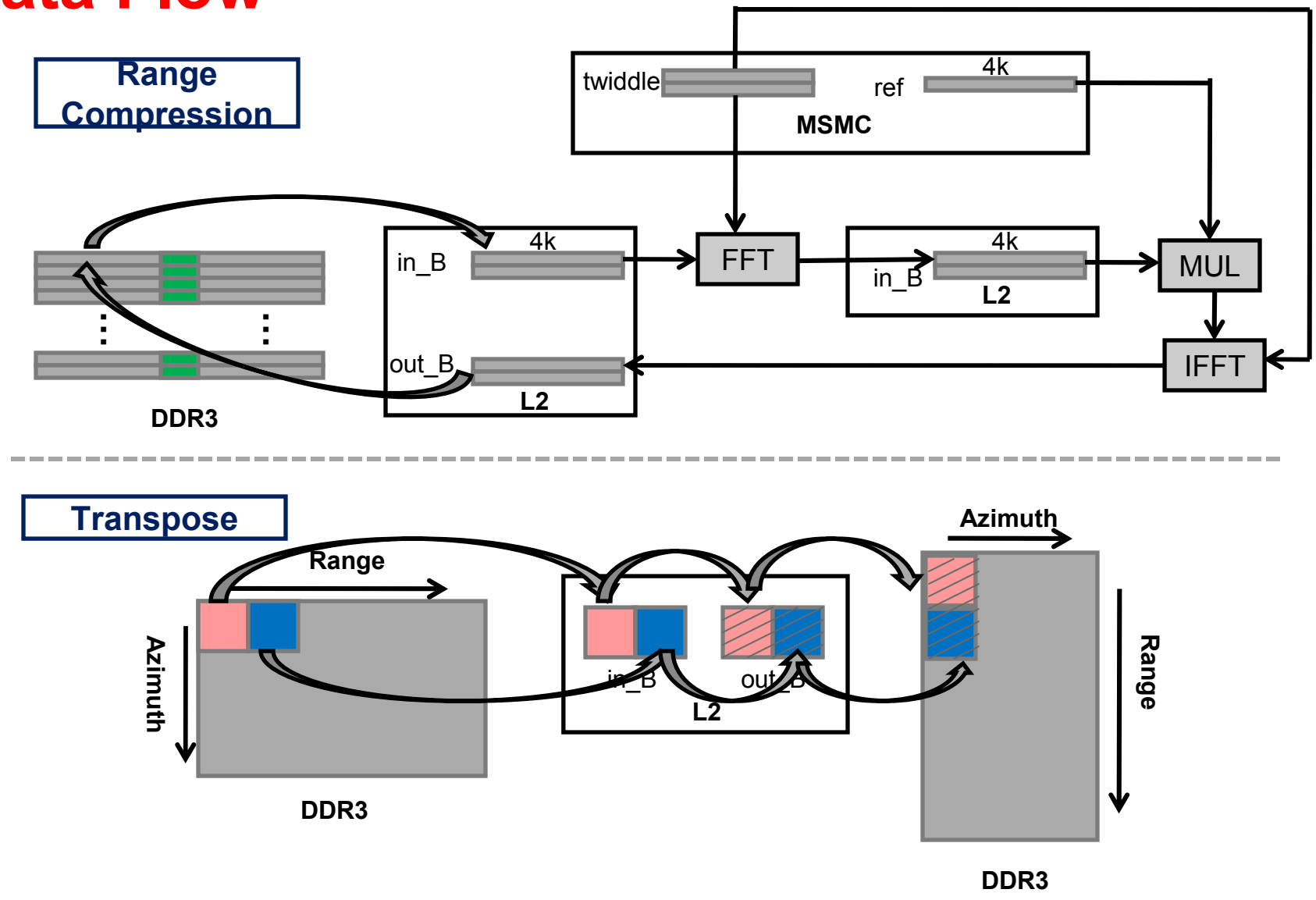




Range-azimuth Algorithm Implementation

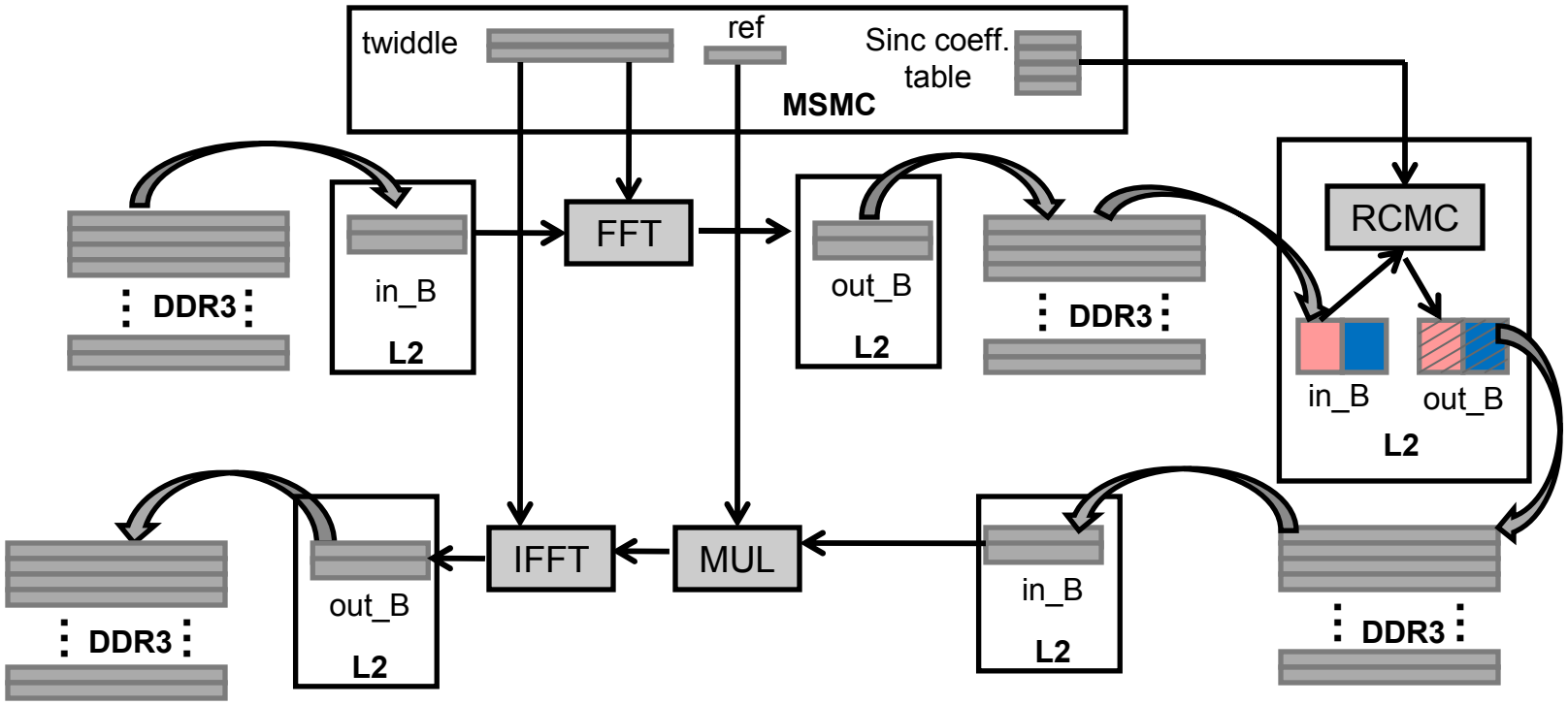


Data Flow



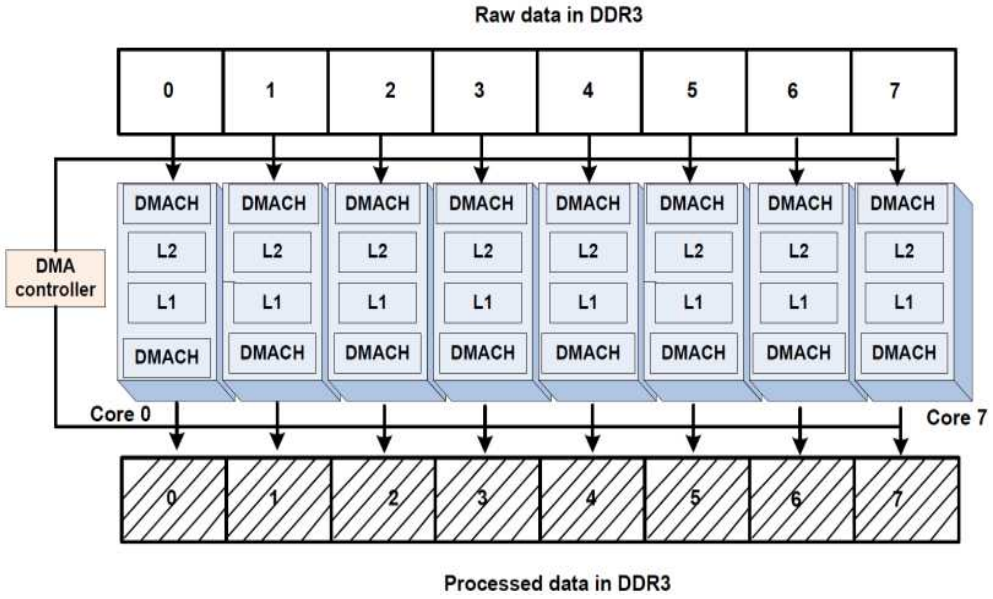
Data Flow

RCMC and Azimuth Compression



Muiticore Mapping

- Allocate memory for each core
- OpenMP for multiple threads running simultaneously
- DMA read from DDR3
- Local processing
- DMA write to DDR3

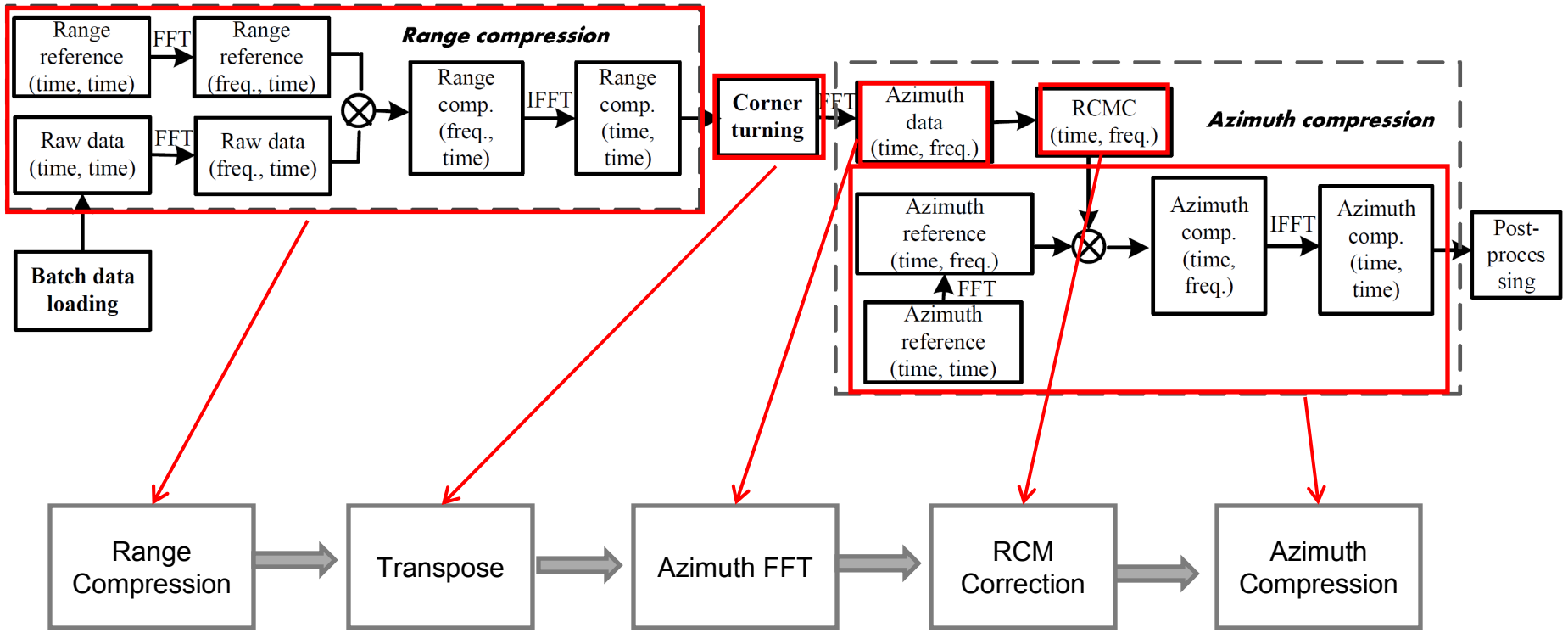


Implementation Profiling

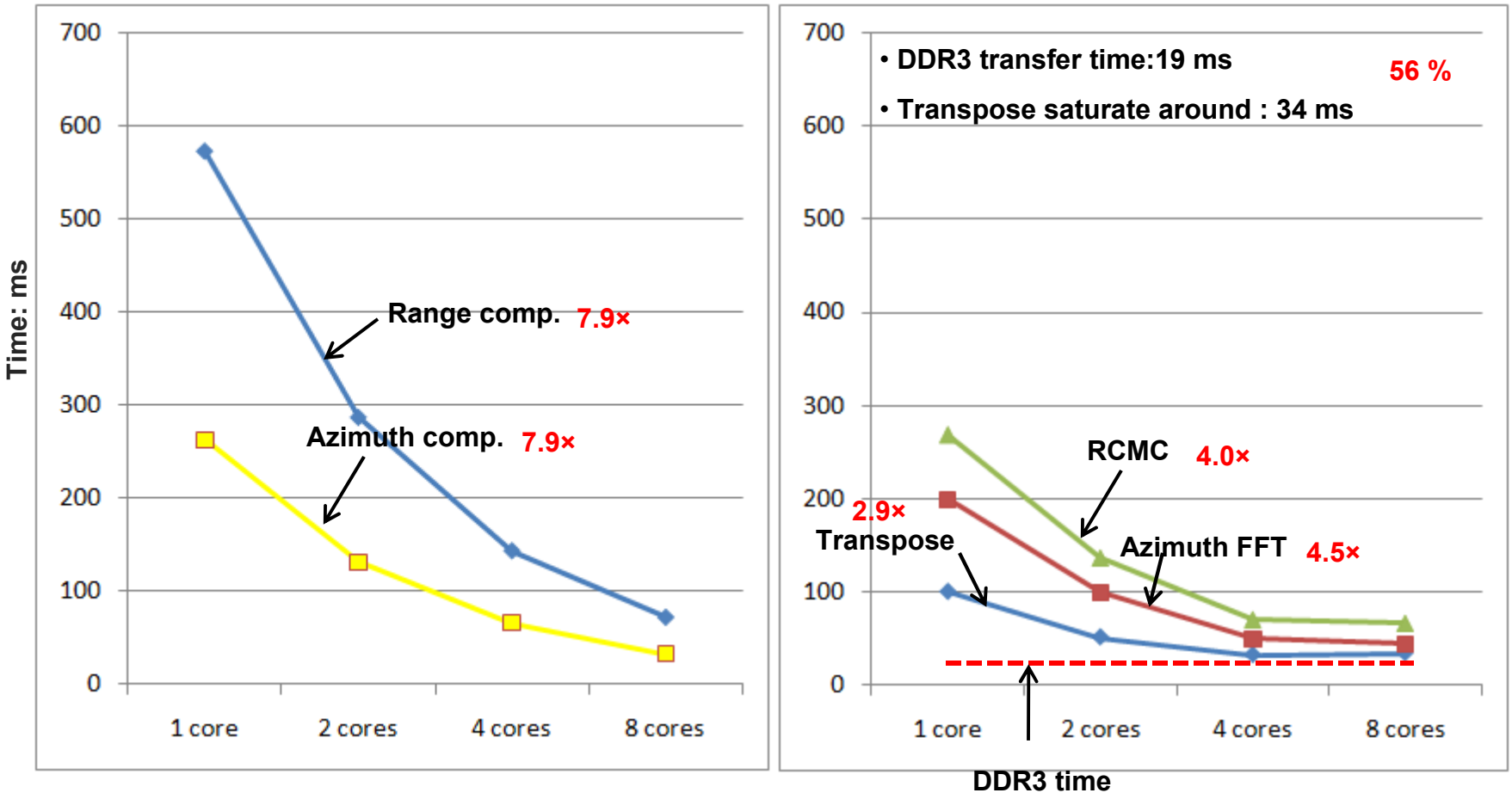
- Setups
  - TMDXEVM6678L
  - Compiler: v7.4.0.A12012
  - OpenMP: v1.0.0.34_eng
  - DSPLIB:v 3.1.0.0, (FFT, complex transpose)
  - L1D cache 32K, L1P cache 32K
  - L2 cache: 128K
  - Data size: 4096*4096, complex single precision

Module Profiling

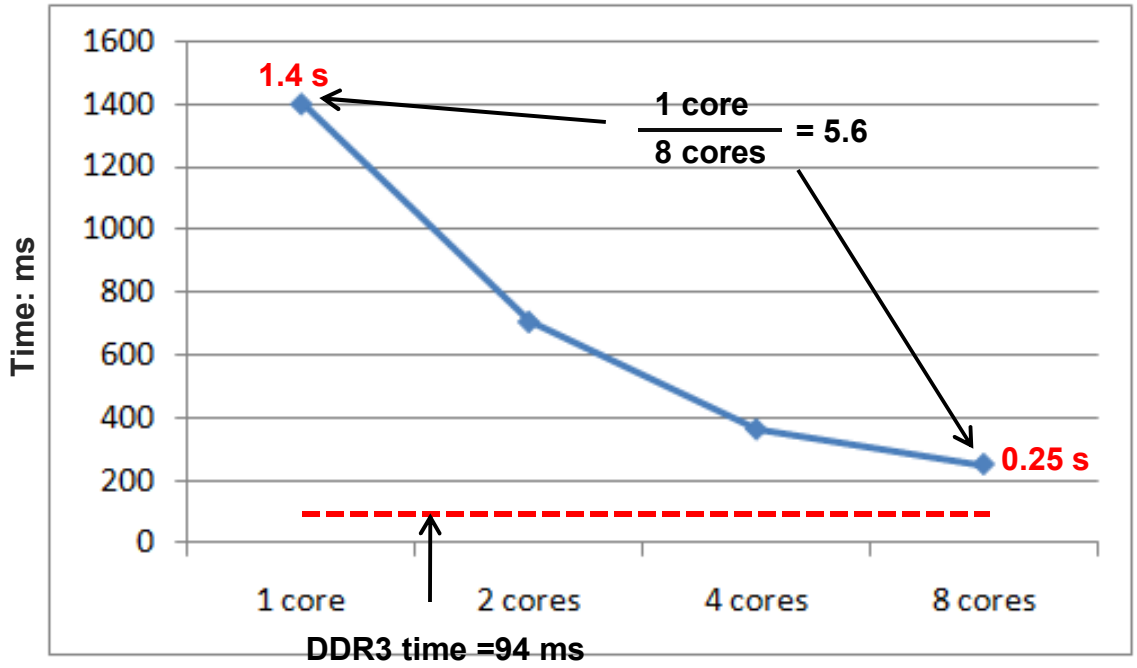
- Five modules



Module Profiling

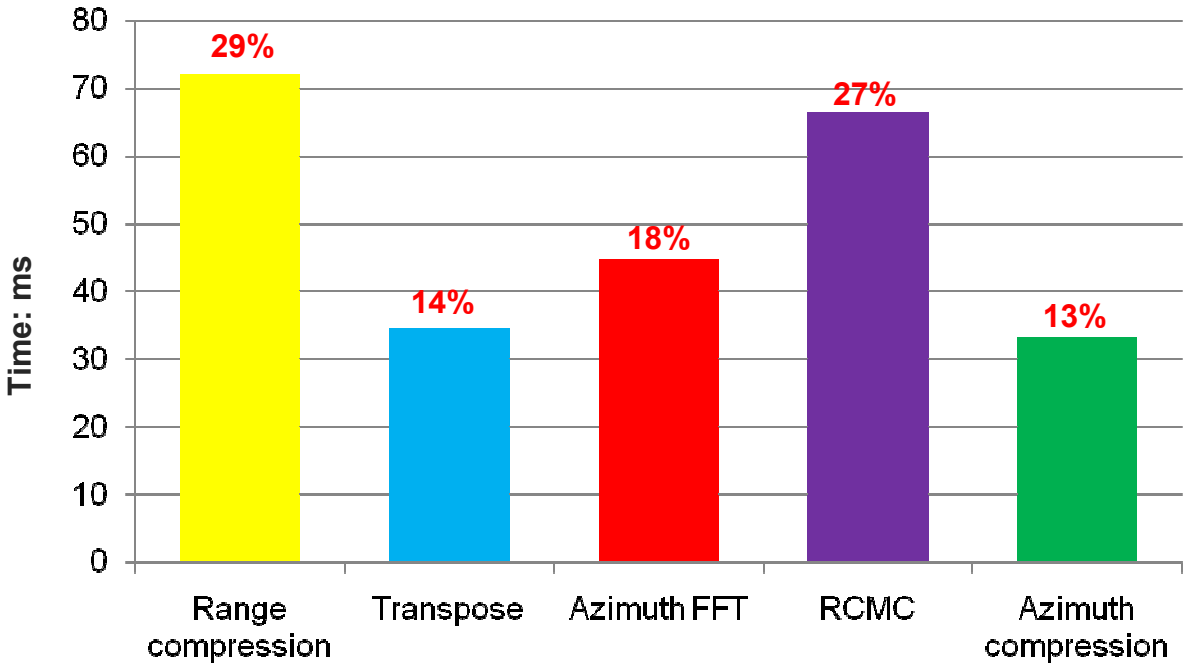


Total Time



$$\frac{94\ \text{ms}}{250\ \text{ms}} = 37.6\%$$

Time Breakdown



Comparison

- GPU benchmark: Nvidia Tesla C1060 (Bisceglie'10)
  - Core clock= 1.296GHz; Processor core #=240; memory= 4GB @ 800MHz
  - Testing algorithm: Range-azimuth algorithm, FFT size 4096
- FPGA: Xilinx VIRTEX-5 (Pfitzner'11)
- Comparison

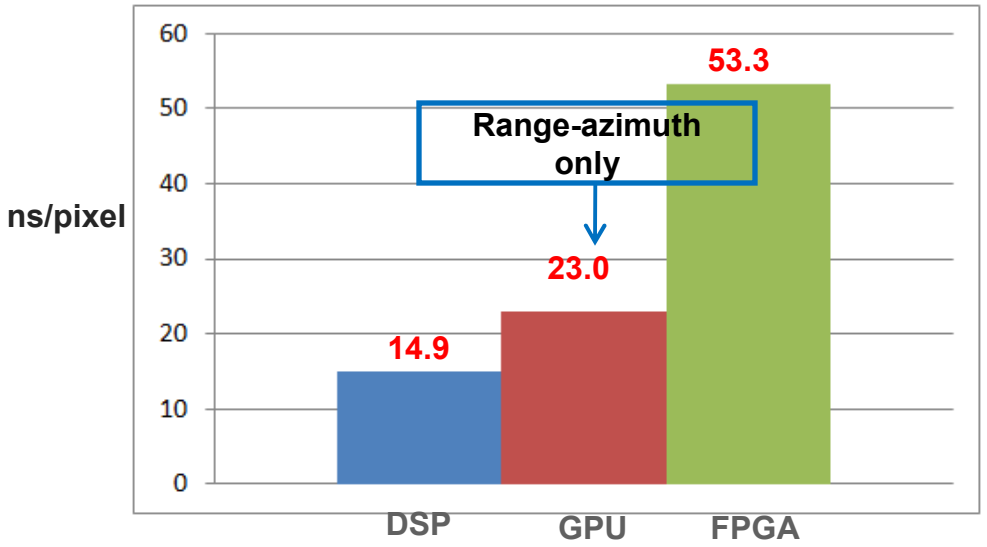
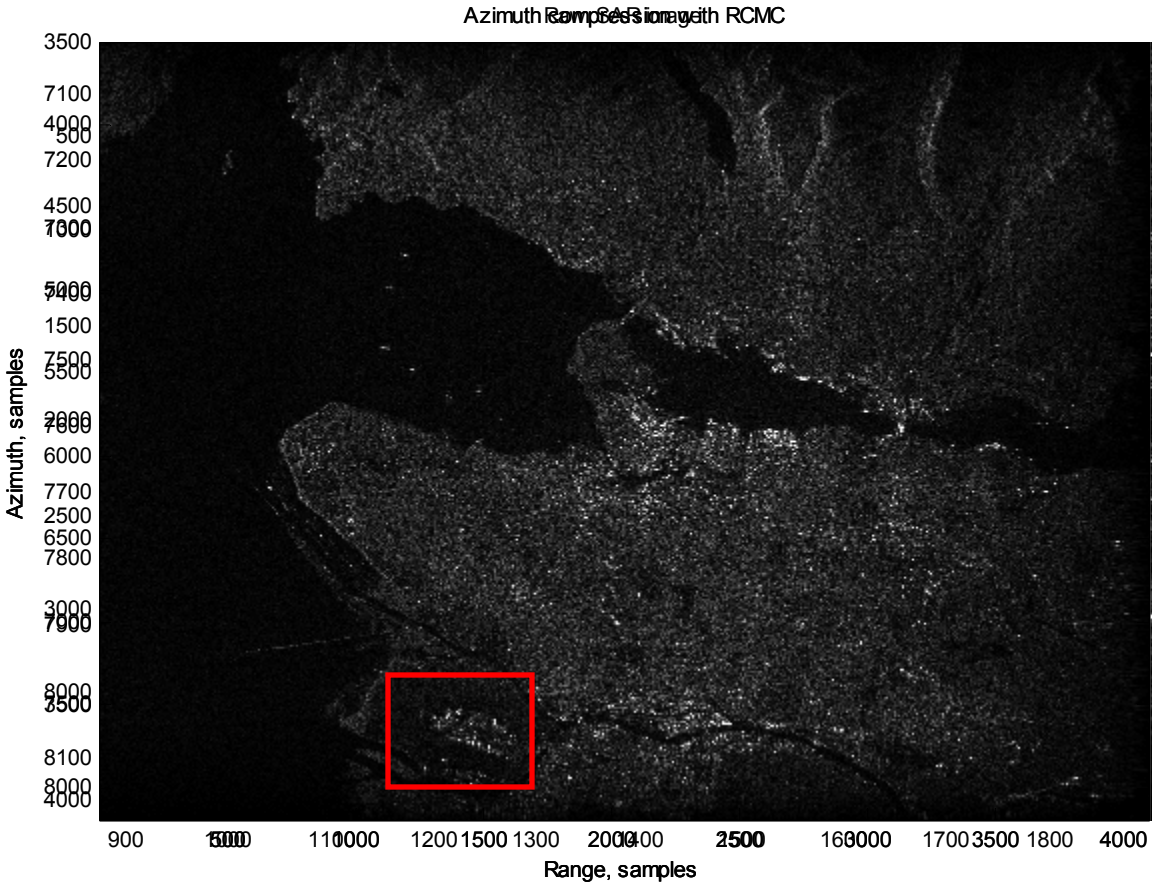


Image Example



RADARSAT: 38km*23km

Conclusions

- Contributions
  - Implementation of range-azimuth algorithm for SAR on TMS320C6678
  - Parallel processing on multiple DSP cores
  - Provide benchmark results for a typical 4k by 4k SAR image
  - Achieve real-time performance with 4 frames/sec
- Next steps
  - Extra modules
    - Doppler parameter estimation, geometry information
    - Auto focusing, computational intensive
  - Larger size FFT (>4K)
  - Evaluation with 4 DSPs connected to server with PCIe

Thanks & Questions