**Efficient Gbit/s Data Transceivers Designed for Verification and SoC Integration**

High performance computing systems generate extreme amounts of data that must be reliably transported between chips and modules. While SERDES research, including that of the author, continues to demonstrate extraordinary data rates per channel, practical interfaces do not approach these limits, but rather find the sweet spot where circuit complexity, power and area start to increase faster than the data rate. System designers then take advantage of advances in packaging that allow highly parallel optical or electrical links, where power and silicon area per Gbps can be more important than the data rate per link.

This presentation describes a transceiver design that has evolved through the implementation and testing of a number of massively parallel communication and imaging systems, with a focus on optimizing system cost, robustness, and time to market. Based on circuits developed in 2001 for a 16 Gbps link that required 69mW/Gbps and 3mm^2 due to the complex equalization needed, performance has scaled with process technology to links with simpler equalization that only require 2mW/Gbps and fit under the SERDES pads.

Synchronization circuits are presented that simplify the chip-level design.
Retiming circuits cross clock domains from digital system clocks to transceiver clocks without the need for expensive FIFOs. Quarter or eighth bit-rate clocks are distributed to minimize power and obviate the need for a PLL for each link. Duty cycle correcting block buffers allow clocks to be driven across long chips without degradation.

First silicon success is paramount in large systems-on-chips where digital design effort, power and area often dwarf that of the data transceivers.
Toward this end, transmit equalization is used, providing eye openings that can be verified with straightforward simulations and measurements, at the expense of slightly larger signal swings to compensate for reduced SNR compared to complex and power-hungry decision feedback equalization (DFE).
Real value behavioral models of the data transceivers enable event-driven simulation in digital simulations with large digital blocks to ensure proper control and port configuration. The portable syntax used in the behavioral models is presented, which allows the models to be verified in analog (SPICE-based) simulators, ensuring accurate correspondence between the models and the transistor-level link designs. Finally, guidelines for chip and board layout are discussed, which, along with design reviews by transceiver designers, help maintain healthy design margins.

The circuits described allow high performance, complex systems to be designed with robust and efficient data transceivers. The verification and integration methodology minimizes the risk of SERDES performance issues, and allows the focus to remain on digital processing and system design.